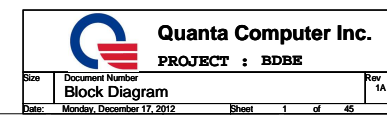
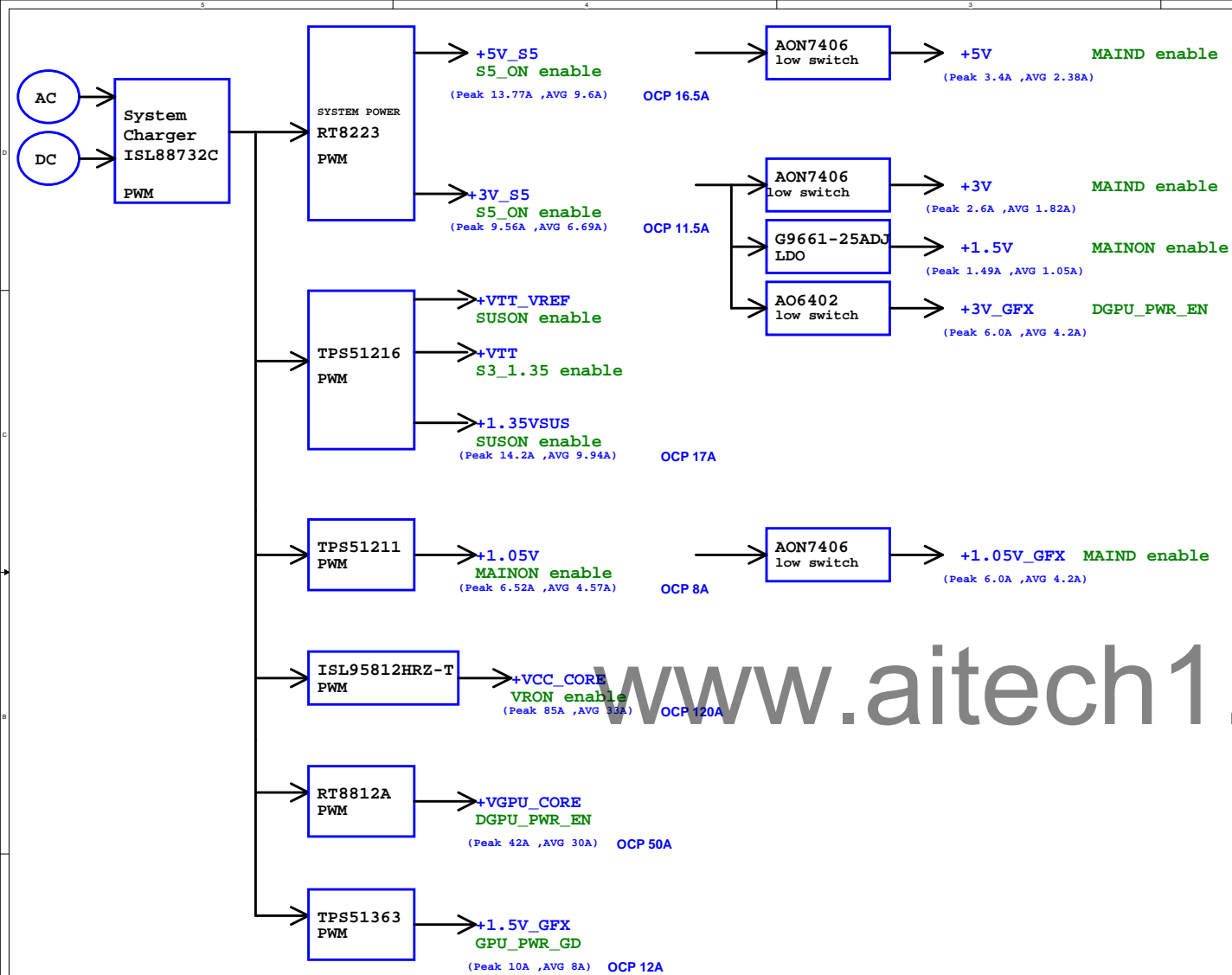


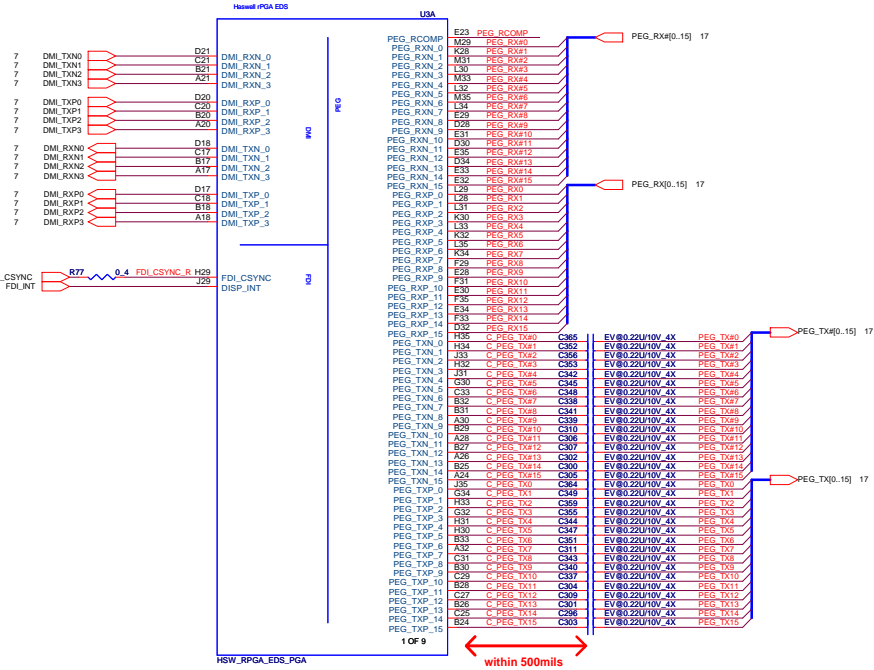
01



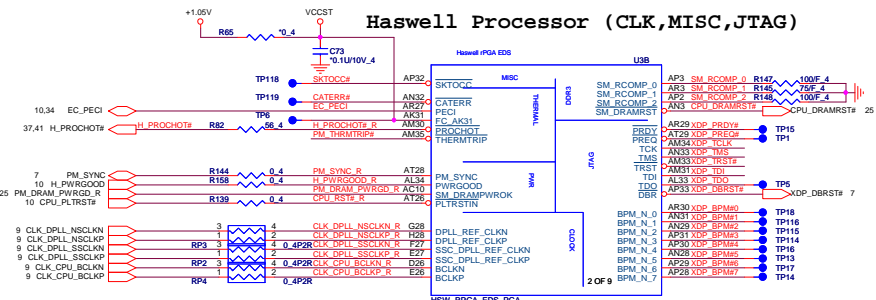


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.5V	+1.5V	MAIN_ON	S0
+1.35V_SUS	+1.35V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+1.05V	+1.05V	MAIN_ON	S0

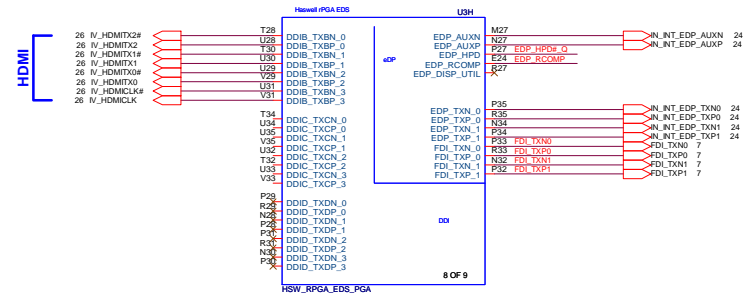
Haswell Processor (DMI,PEG,FDI)



```
Haswell Processor (CLK,MISC,JTAG)
```



Haswell Processor (DDI,eDP,FDI)



within 500mils

ESD Solution reserve

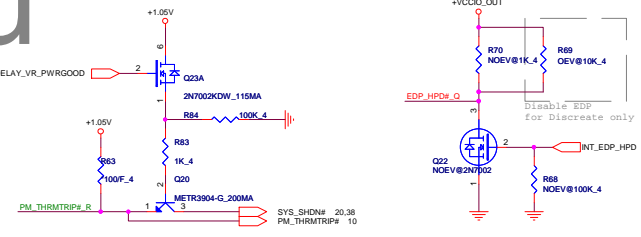
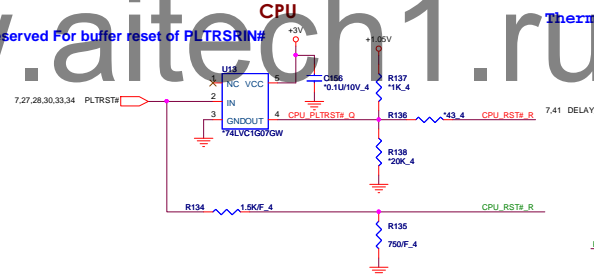
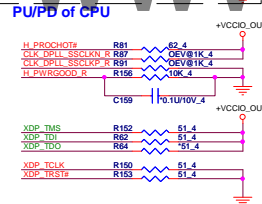
Reserved For buffer reset of PLTRSRIN#

Thermal Trip & Process HOT CPU

eDP Hot Plug Detect CPU

FDI Disabling (Discrete Only)
<CPU>

DP & PEG Compensation



Disable EDP
for Discreate only

INT_EDP_HPD 24,27

 R68

CDI TERM

 S5_ON 34,38

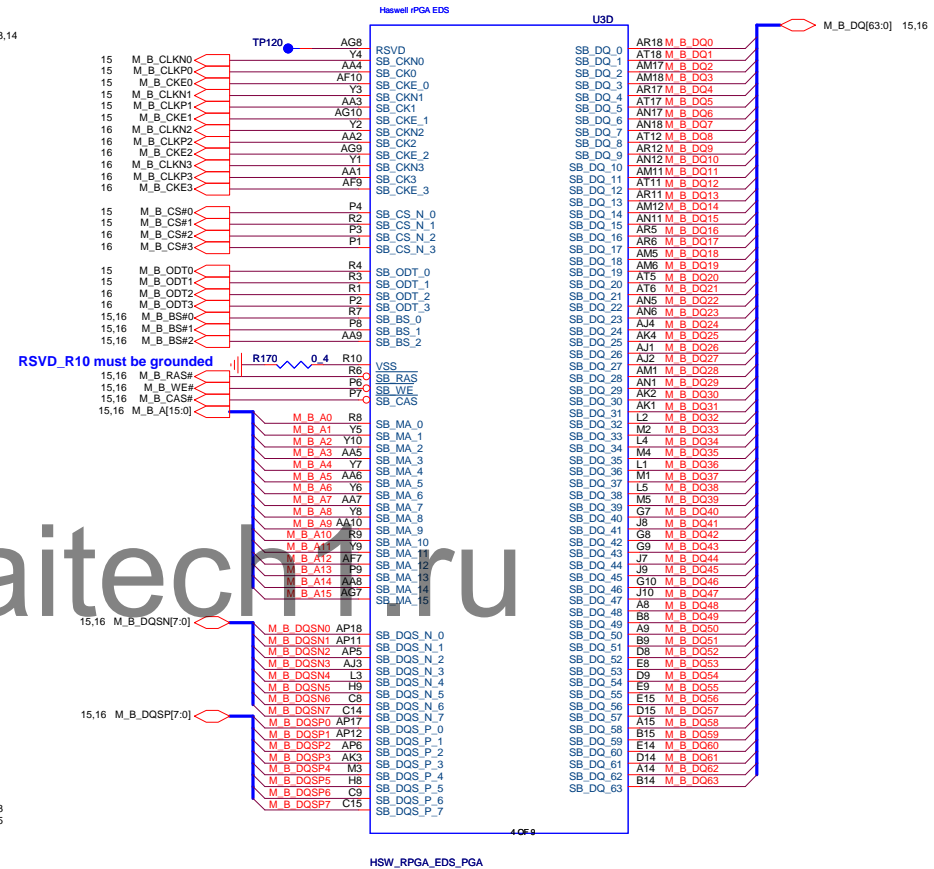
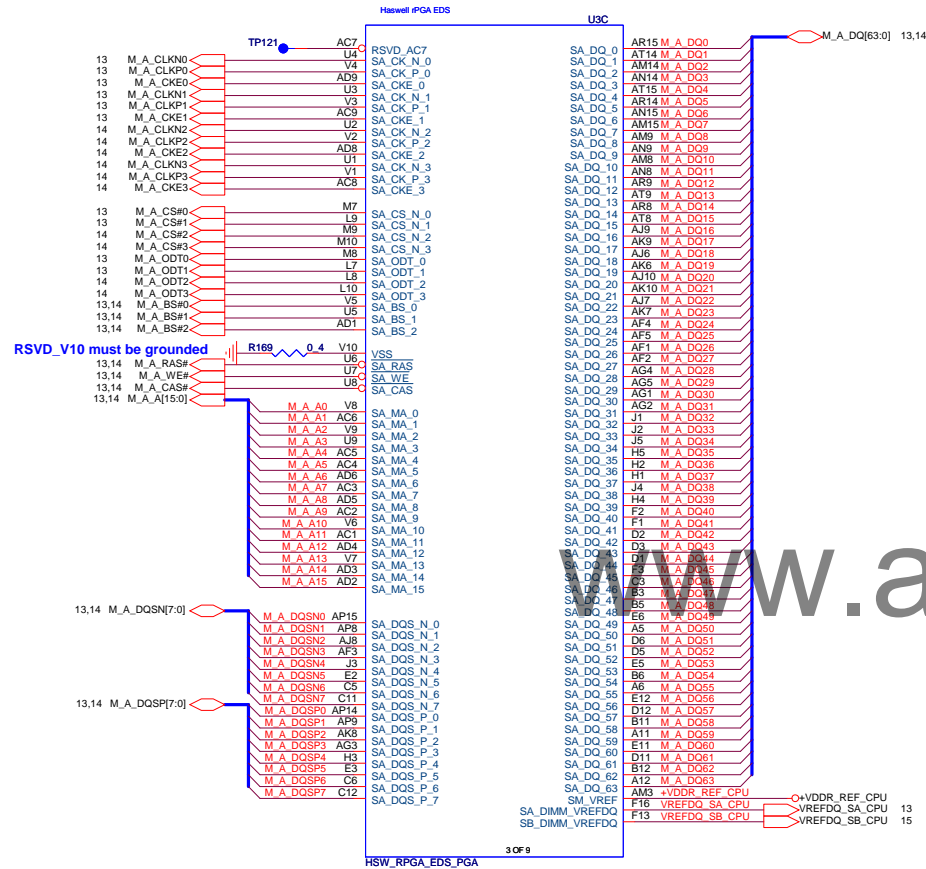
D4 *1SS355_100MA +3VPCU

CT • BDRF

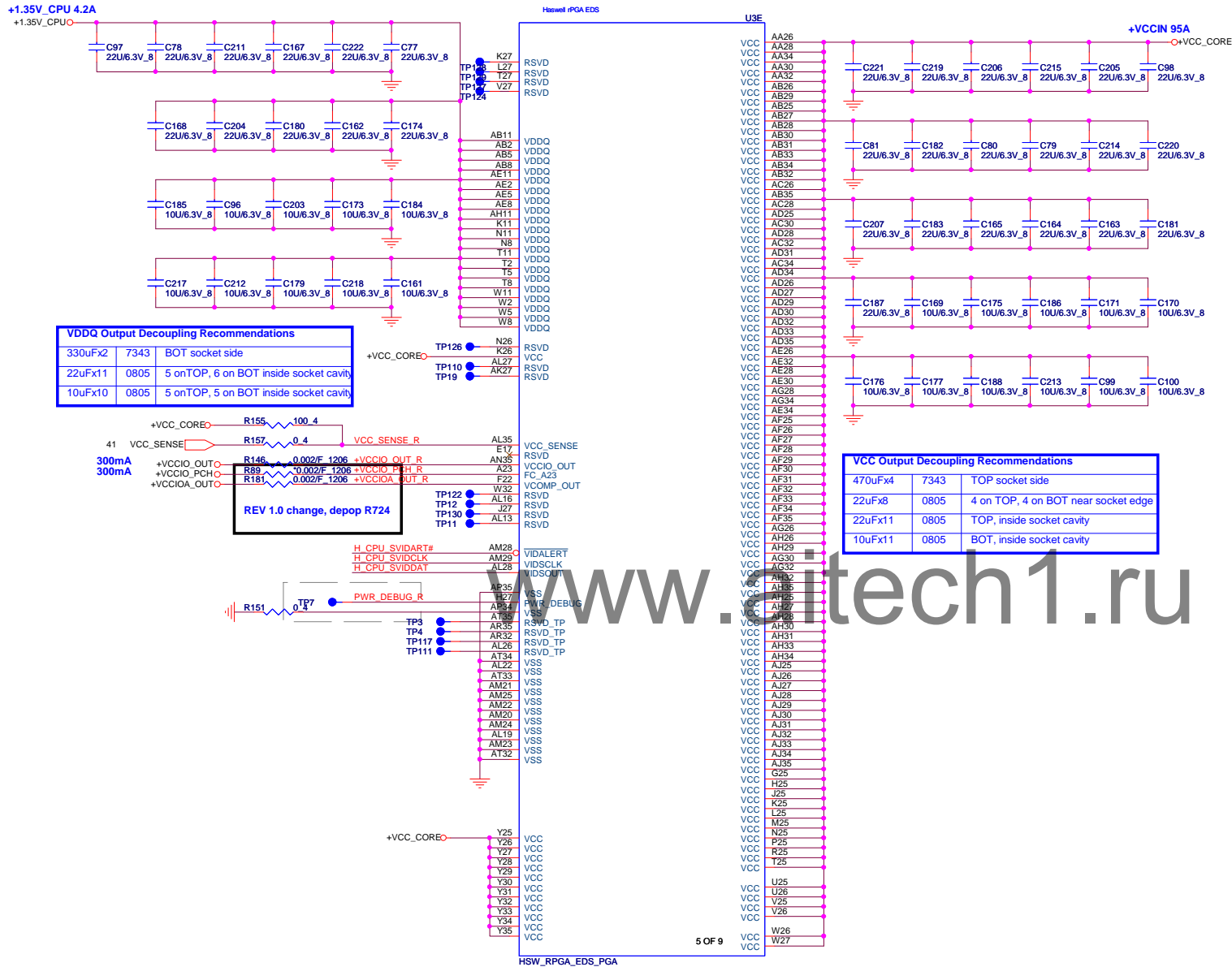
PEG/DMI/FDI)

Price 9 91 40

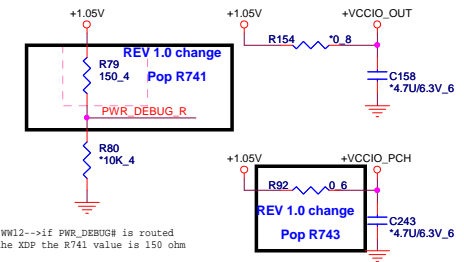
Haswell Processor (DDR3)



Haswell Processor (POWER)

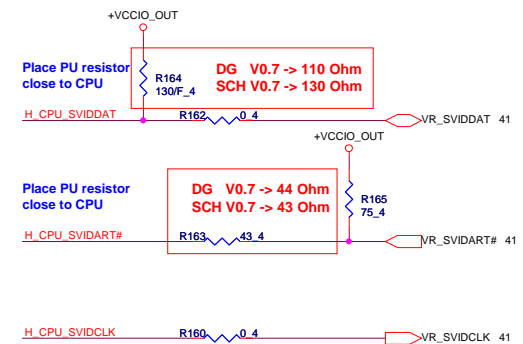


Power Test Propose



SVID

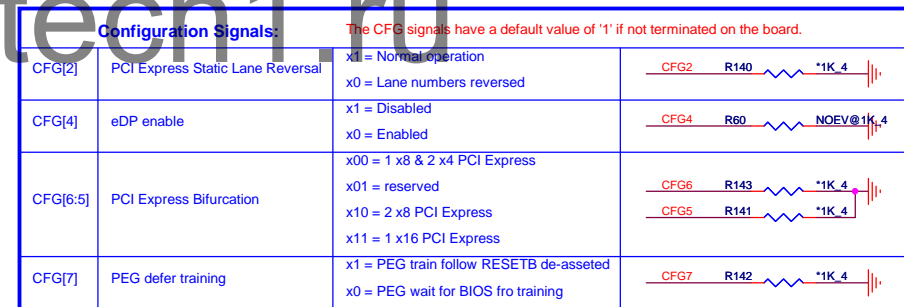
Layout note: need routing together and ALERT need between CLK and DATA.



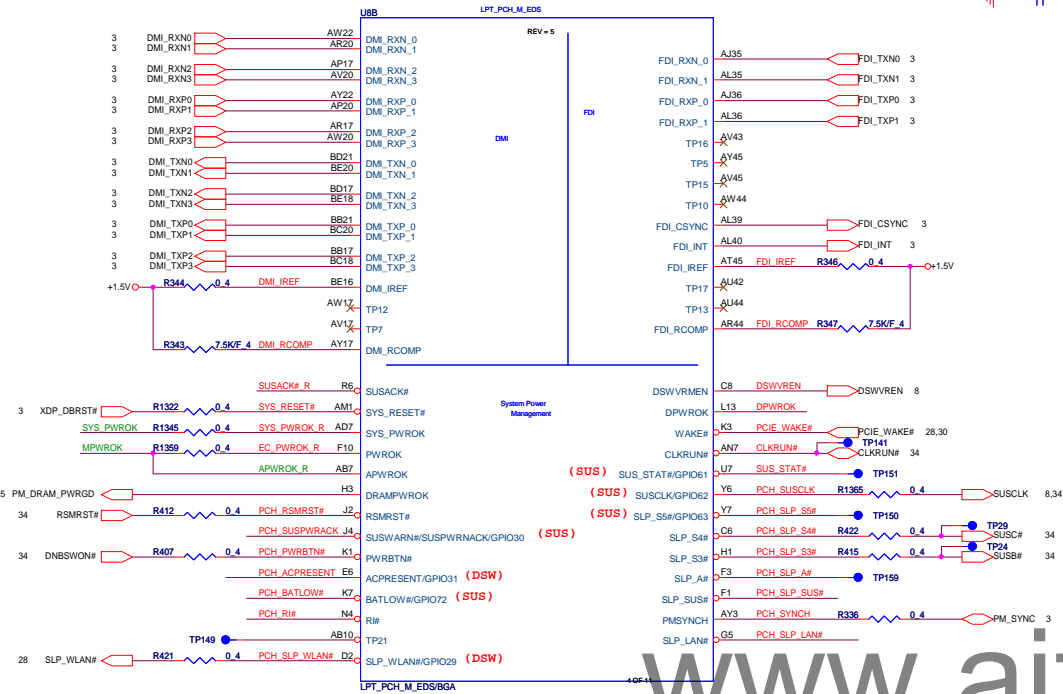
Quanta Computer Inc.

PROJECT : BDDE

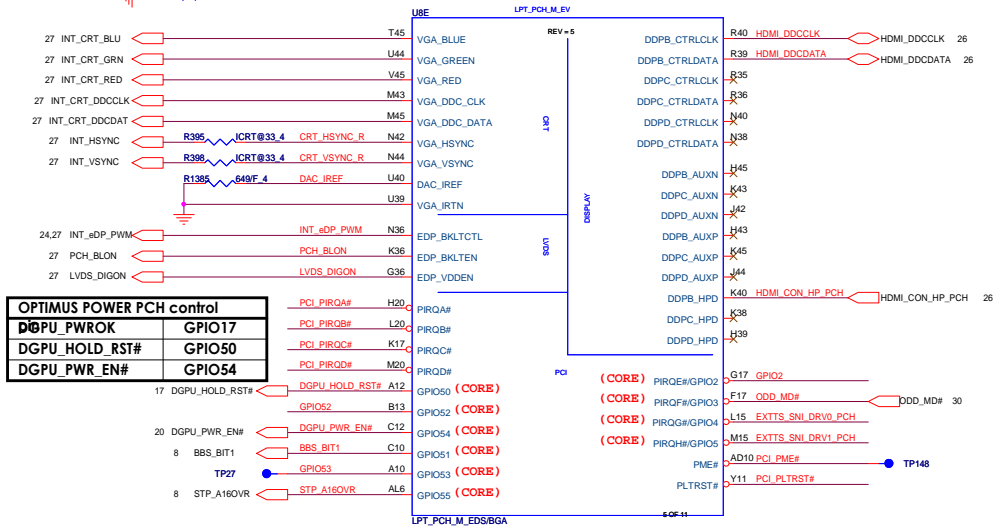
Size Document Number
Haswell 4/5 (POWER)
Date: Monday, December 17, 2012 Sheet 5 of 45



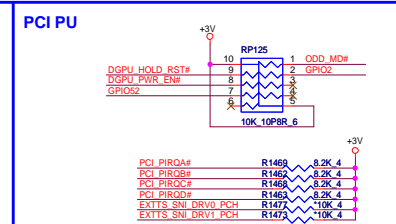
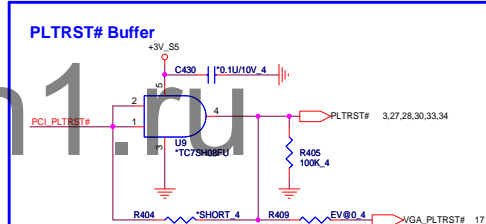
Lynx Point (DMI,FDI,PM)



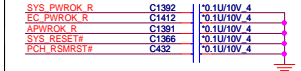
Lynx Point (CRT,PCI,DDI CNTL)



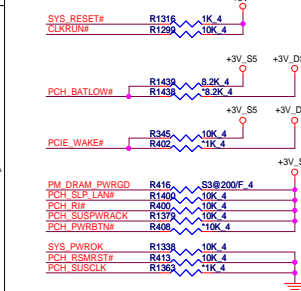
OPTIMUS POWER PCH control	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54



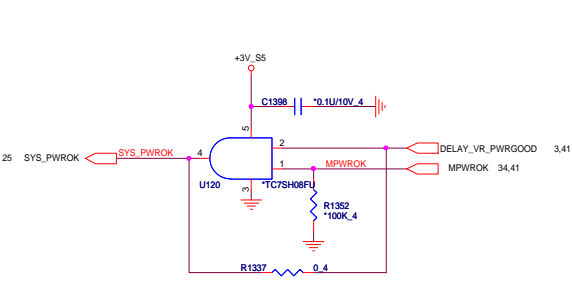
ESD Solution reserve



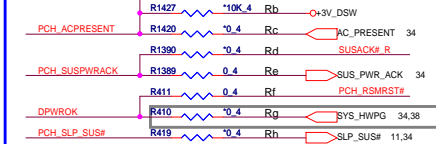
PCH PM PU/PD



SYSPWOK

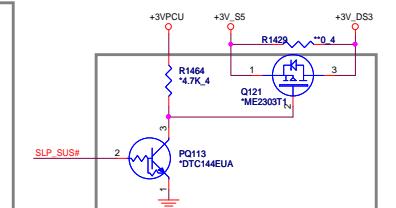
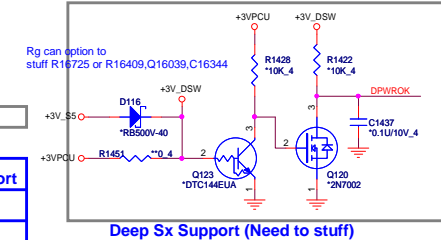


DSW Circuit



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

DS Power

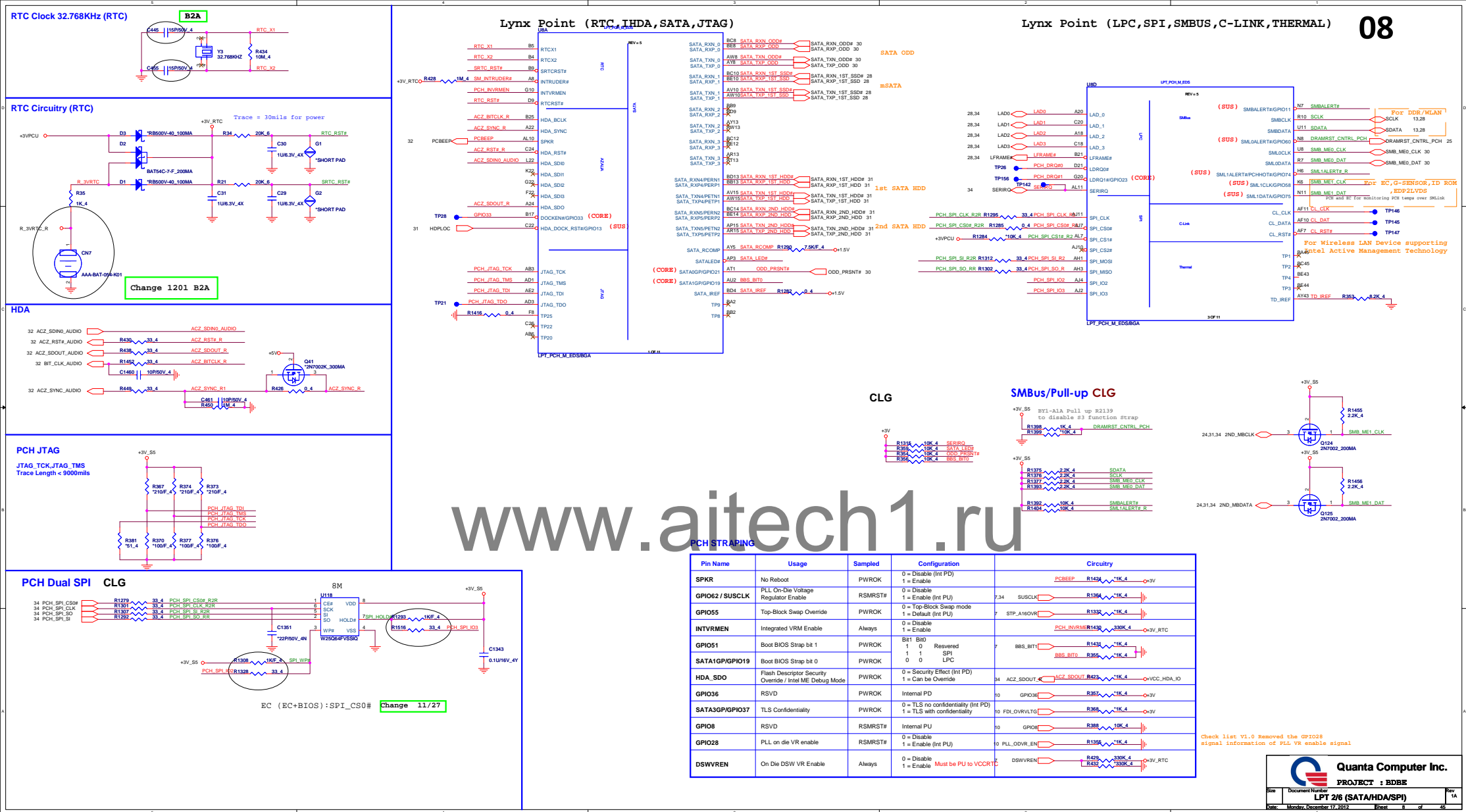


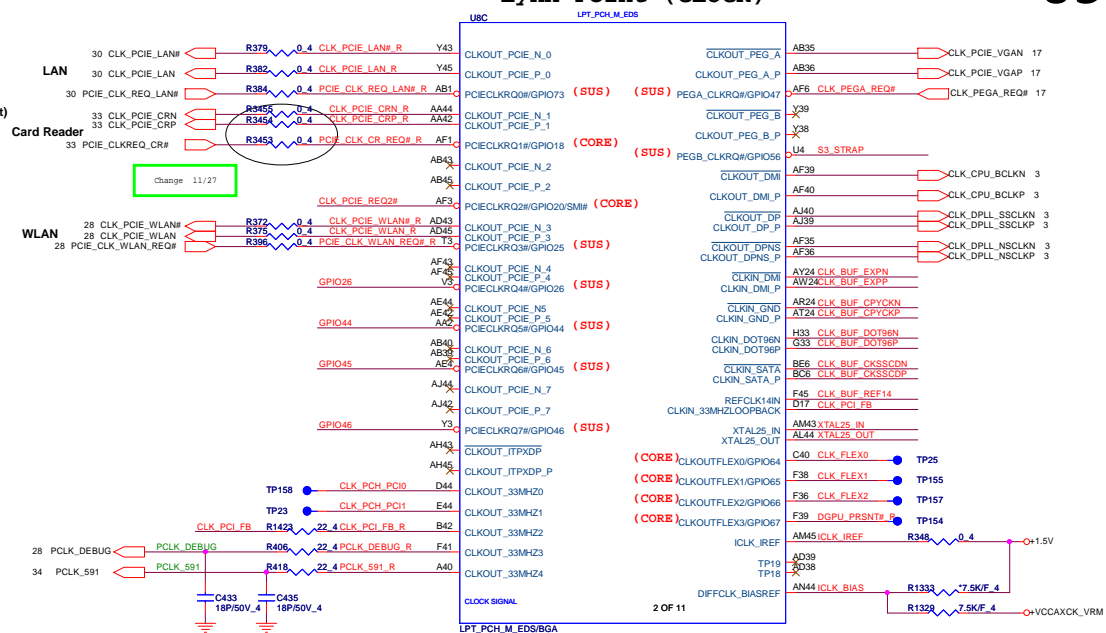
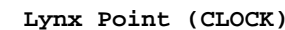
Deep Sx Support (Need to stuff)



Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number LPT 1/6 (DMI/FDI/VGA)	Rev 1A
Date:	Monday, December 17, 2012	Sheet 7 of 45



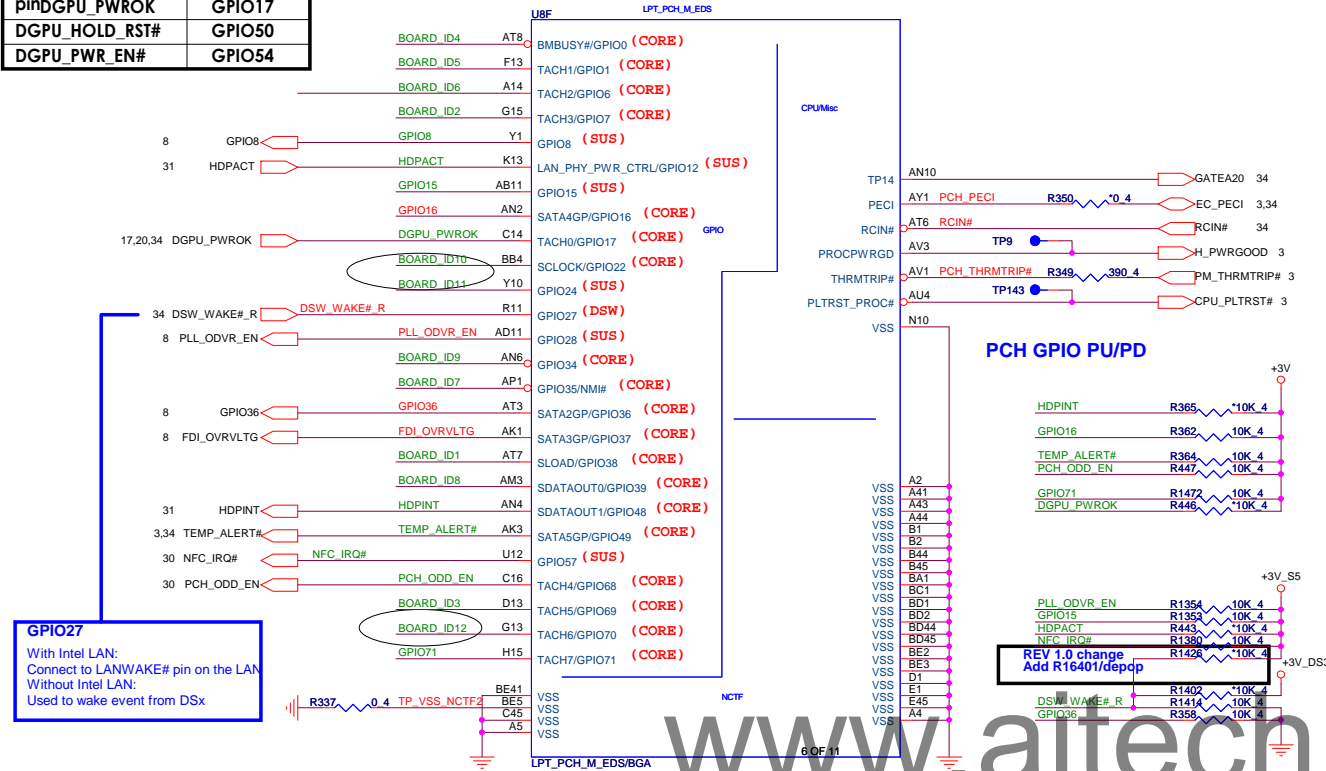


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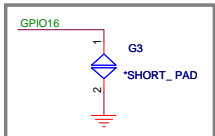
OPTIMUS POWER PCH control	
pinDGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

Lynx Point (GPIO,CPU/MISC,NCTF)



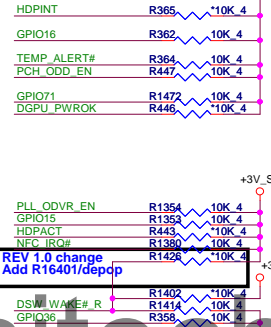
GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

PU & Password Clear

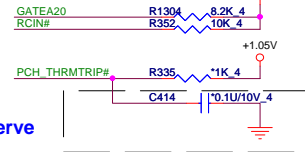


REV-B2A Add G3 for Clear CMOS password

PCH GPIO PU/PD



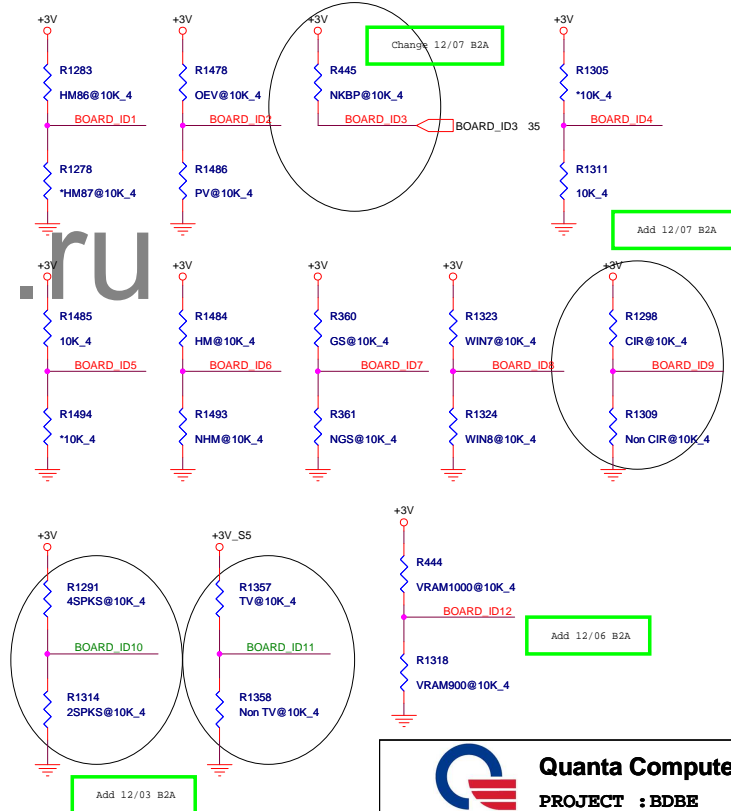
PCH MISC PU/PD



ESD Solution Reserve

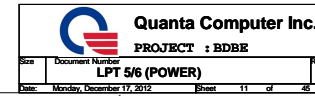
BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
UMA Discrete				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
W/ CIR W/O CIR									H L			
4 SPKS 2 SPKS											H L	
TV SKU SSD SKU												H L
VRAM 1000 VRAM 900												H L



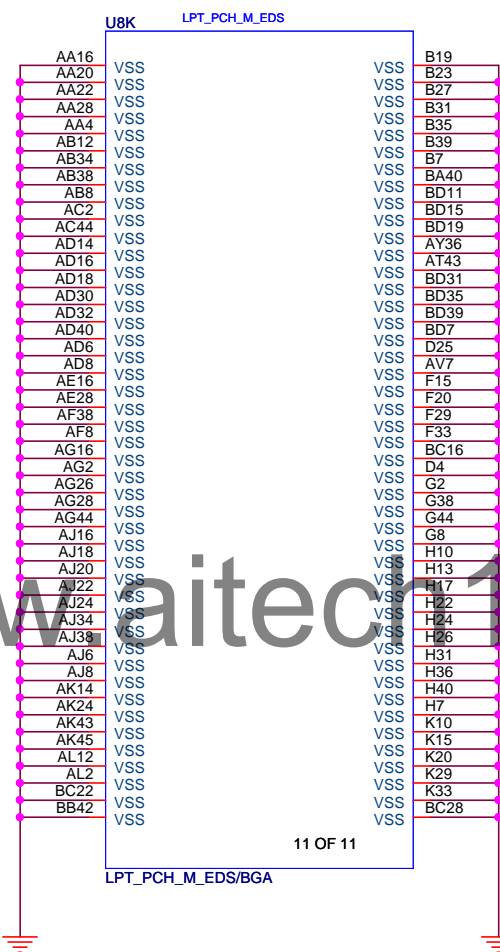
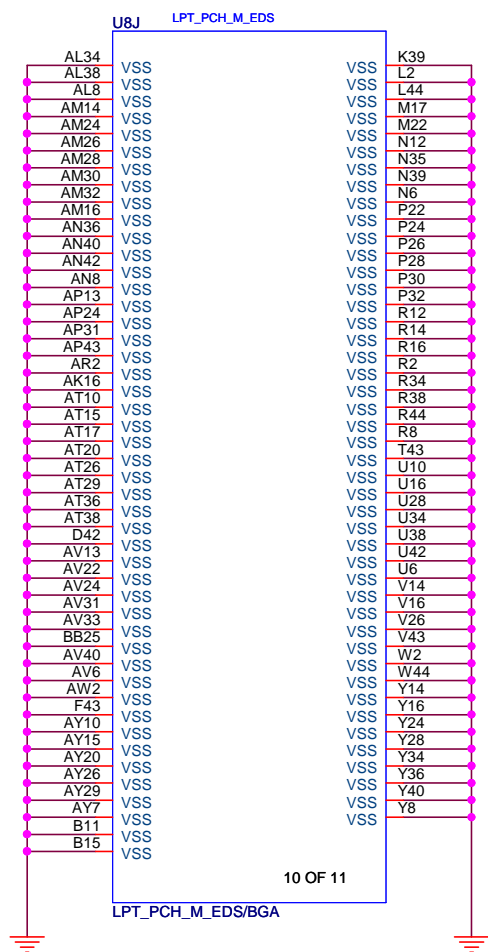
Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
Date:	Monday, December 17, 2012	Sheet 10 of 45



Lynx Point (GND)

Lynx Point (GND)




Quanta Computer Inc.

PROJECT : BDBE

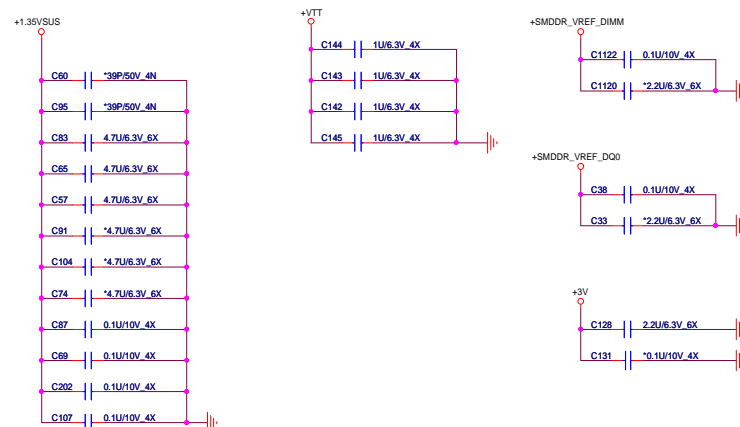
Size	Document Number	Rev
	LPT 6/6 (GND)	1A
Date:	Monday, December 17, 2012	Sheet 12 of 45



 Quanta Computer Inc. PROJECT : DBDE	
Size	Document Number System Memory 1/2 (5.2H)
Date: Monday, December 17, 2012	Sheet 13 of 45

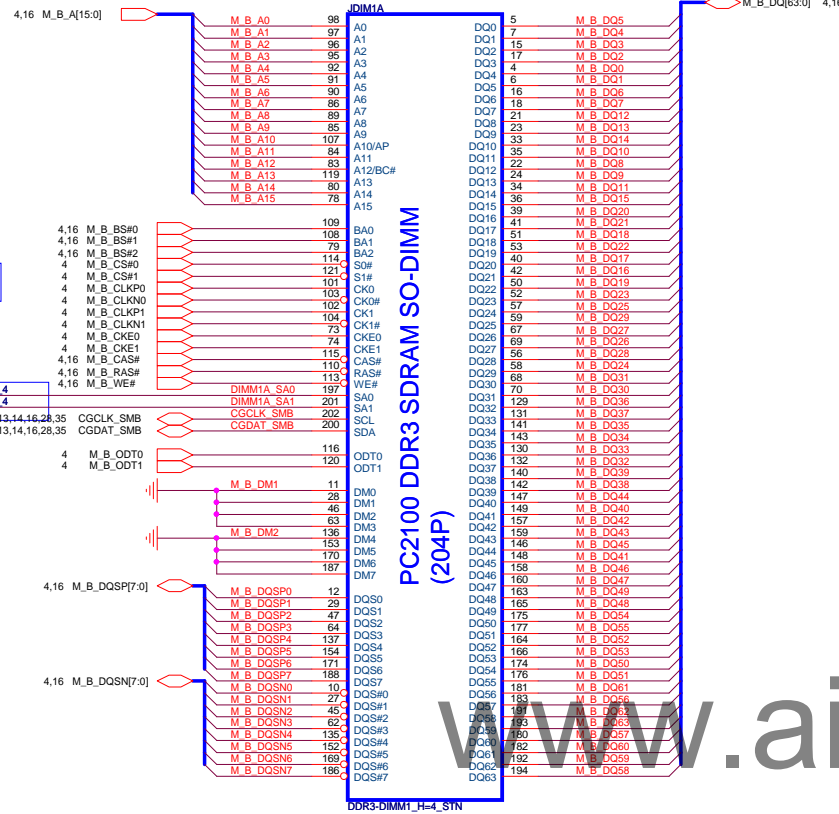
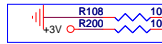


ESD Solution Reserve

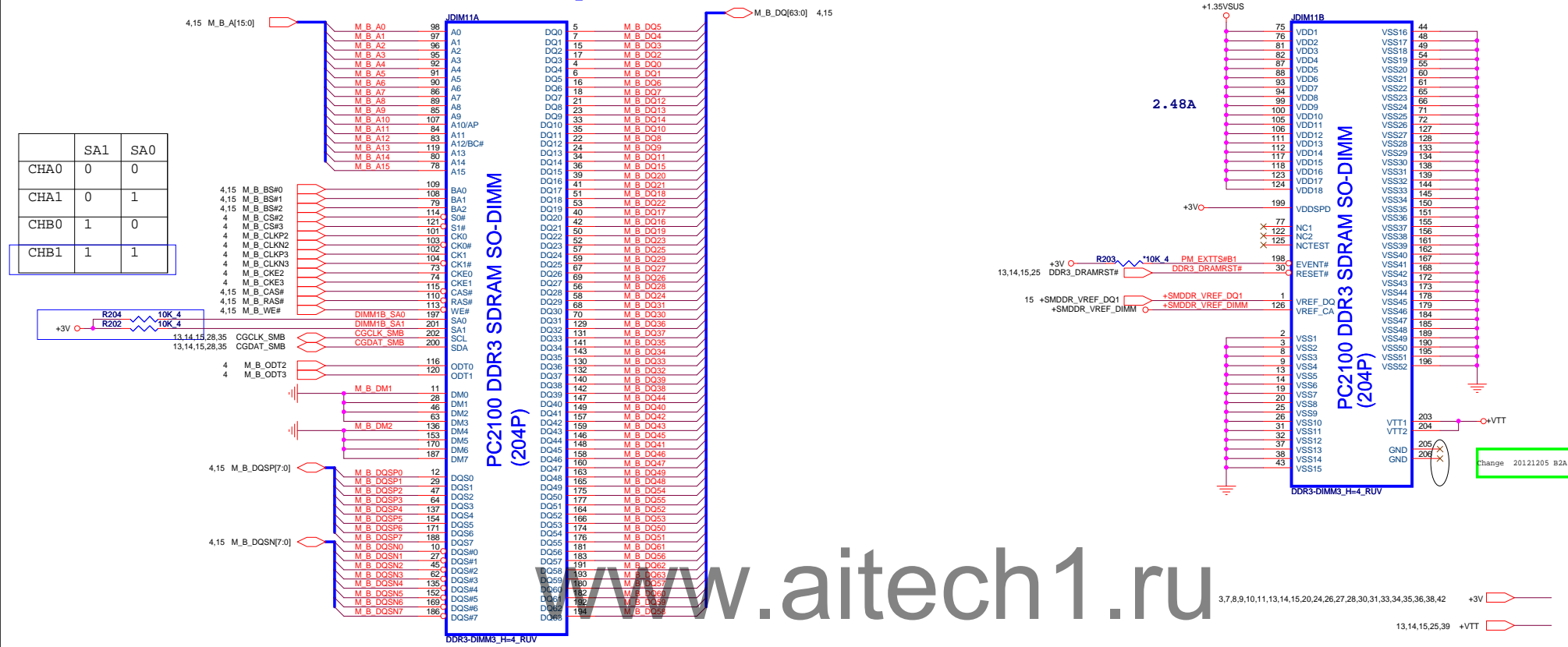


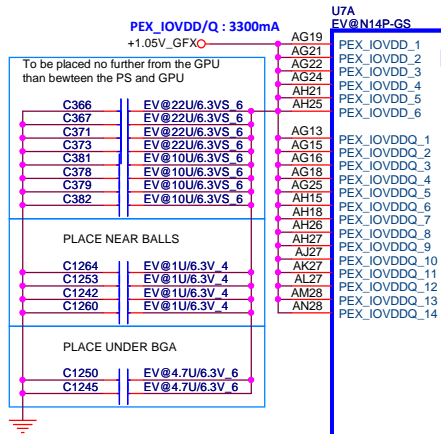
BOT Side Far away CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



TOP Side Far away CPU





[PEG Interface]

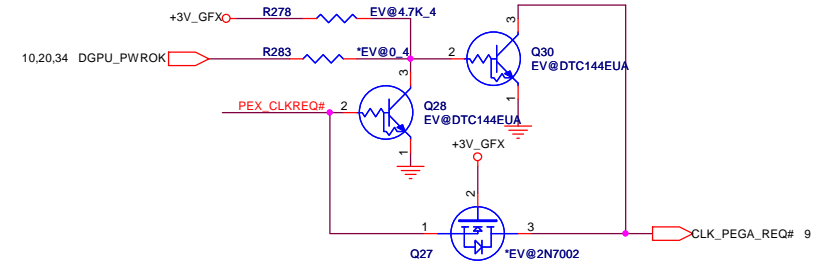
U7A
EV@N14P-GS

AG19	PEX_IOVDD_1
AG21	PEX_IOVDD_2
AG22	PEX_IOVDD_3
AG24	PEX_IOVDD_4
AH21	PEX_IOVDD_5
AH25	PEX_IOVDD_6
AG13	PEX_IOVDDQ_1
AG15	PEX_IOVDDQ_2
AG16	PEX_IOVDDQ_3
AG18	PEX_IOVDDQ_4
AG25	PEX_IOVDDQ_5
AH15	PEX_IOVDDQ_6
AH18	PEX_IOVDDQ_7
AH26	PEX_IOVDDQ_8
AH27	PEX_IOVDDQ_9
AJ27	PEX_IOVDDQ_10
AK27	PEX_IOVDDQ_11
AL27	PEX_IOVDDQ_12
AM28	PEX_IOVDDQ_13
AN28	PEX_IOVDDQ_14

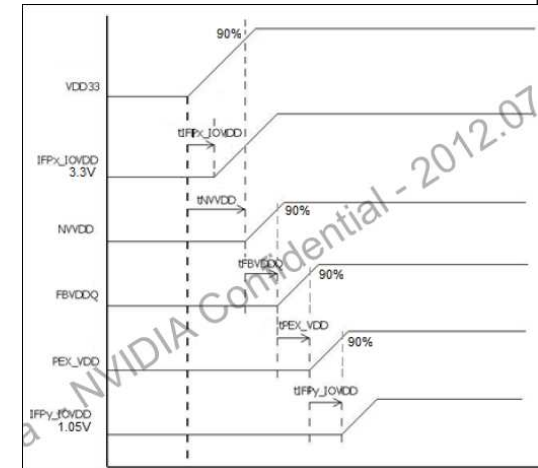
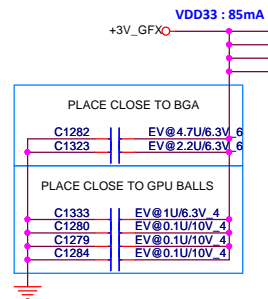
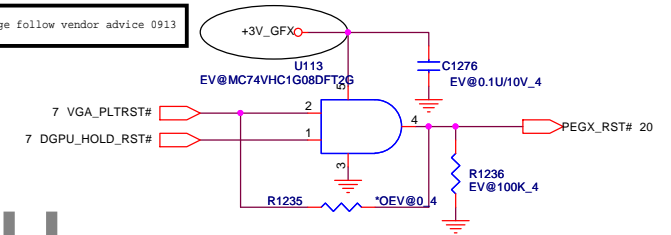
PEX_RX0	AN12	PEG_TX0	3
PEX_RX0_N	AN12	PEG_TX0#	3
PEX_RX1	AM14	PEG_TX1	3
PEX_RX1_N	AP14	PEG_TX1#	3
PEX_RX2	AP15	PEG_TX2	3
PEX_RX2_N	AN15	PEG_TX2#	3
PEX_RX3	AM15	PEG_TX3	3
PEX_RX3_N	AN17	PEG_TX3#	3
PEX_RX4	AP17	PEG_TX4	3
PEX_RX4_N	AN18	PEG_TX4#	3
PEX_RX5	AP18	PEG_TX5	3
PEX_RX5_N	AN18	PEG_TX5#	3
PEX_RX6	AM20	PEG_TX6	3
PEX_RX6_N	AP20	PEG_TX6#	3
PEX_RX7	AN21	PEG_TX7	3
PEX_RX7_N	AM21	PEG_TX7#	3
PEX_RX8	AP21	PEG_TX8	3
PEX_RX8_N	AN21	PEG_TX8#	3
PEX_RX9	AM22	PEG_TX9	3
PEX_RX9_N	AP22	PEG_TX9#	3
PEX_RX10	AN23	PEG_TX10	3
PEX_RX10_N	AM23	PEG_TX10#	3
PEX_RX11	AP23	PEG_TX11	3
PEX_RX11_N	AN24	PEG_TX11#	3
PEX_RX12	AM24	PEG_TX12	3
PEX_RX12_N	AP24	PEG_TX12#	3
PEX_RX13	AN26	PEG_TX13	3
PEX_RX13_N	AM26	PEG_TX13#	3
PEX_RX14	AP26	PEG_TX14	3
PEX_RX14_N	AN27	PEG_TX14#	3
PEX_RX15	AM27	PEG_TX15	3
PEX_RX15_N	AP27	PEG_TX15#	3

AK14	C PEG_RX0	C1203	EV@0.22U/10V	4	PEG_RX0	3
AJ14	C PEG_RX#0	C1206	EV@0.22U/10V	4	PEG_RX#0	3
AH14	C PEG_RX1	C1219	EV@0.22U/10V	4	PEG_RX1	3
AG14	C PEG_RX#1	C1223	EV@0.22U/10V	4	PEG_RX#1	3
AK15	C PEG_RX2	C1208	EV@0.22U/10V	4	PEG_RX2	3
AJ15	C PEG_RX#2	C1209	EV@0.22U/10V	4	PEG_RX#2	3
AL16	C PEG_RX3	C1211	EV@0.22U/10V	4	PEG_RX3	3
AK16	C PEG_RX#3	C1213	EV@0.22U/10V	4	PEG_RX#3	3
AK17	C PEG_RX4	C1200	EV@0.22U/10V	4	PEG_RX4	3
AJ17	C PEG_RX#4	C1201	EV@0.22U/10V	4	PEG_RX#4	3
AH17	C PEG_RX5	C1197	EV@0.22U/10V	4	PEG_RX5	3
AG17	C PEG_RX#5	C1199	EV@0.22U/10V	4	PEG_RX#5	3
AK18	C PEG_RX6	C1202	EV@0.22U/10V	4	PEG_RX6	3
AJ18	C PEG_RX#6	C1205	EV@0.22U/10V	4	PEG_RX#6	3
AK19	C PEG_RX7	C1190	EV@0.22U/10V	4	PEG_RX7	3
AJ19	C PEG_RX#7	C1193	EV@0.22U/10V	4	PEG_RX#7	3
AK20	C PEG_RX8	C1195	EV@0.22U/10V	4	PEG_RX8	3
AJ20	C PEG_RX#8	C1194	EV@0.22U/10V	4	PEG_RX#8	3
AH20	C PEG_RX9	C1188	EV@0.22U/10V	4	PEG_RX9	3
AK20	C PEG_RX#9	Q186	EV@0.22U/10V	4	PEG_RX#9	3
AK21	C PEG_RX10	C1183	EV@0.22U/10V	4	PEG_RX10	3
AJ21	C PEG_RX#10	C1177	EV@0.22U/10V	4	PEG_RX#10	3
AK22	C PEG_RX11	C1196	EV@0.22U/10V	4	PEG_RX11	3
AJ22	C PEG_RX#11	C1198	EV@0.22U/10V	4	PEG_RX#11	3
AK23	C PEG_RX12	C1192	EV@0.22U/10V	4	PEG_RX12	3
AJ23	C PEG_RX#12	C1189	EV@0.22U/10V	4	PEG_RX#12	3
AH23	C PEG_RX13	C1182	EV@0.22U/10V	4	PEG_RX13	3
AK23	C PEG_RX#13	C1176	EV@0.22U/10V	4	PEG_RX#13	3
AK24	C PEG_RX14	C1171	EV@0.22U/10V	4	PEG_RX14	3
AJ24	C PEG_RX#14	C1167	EV@0.22U/10V	4	PEG_RX#14	3
AK25	C PEG_RX15	C1174	EV@0.22U/10V	4	PEG_RX15	3
AJ25	C PEG_RX#15	C1172	EV@0.22U/10V	4	PEG_RX#15	3

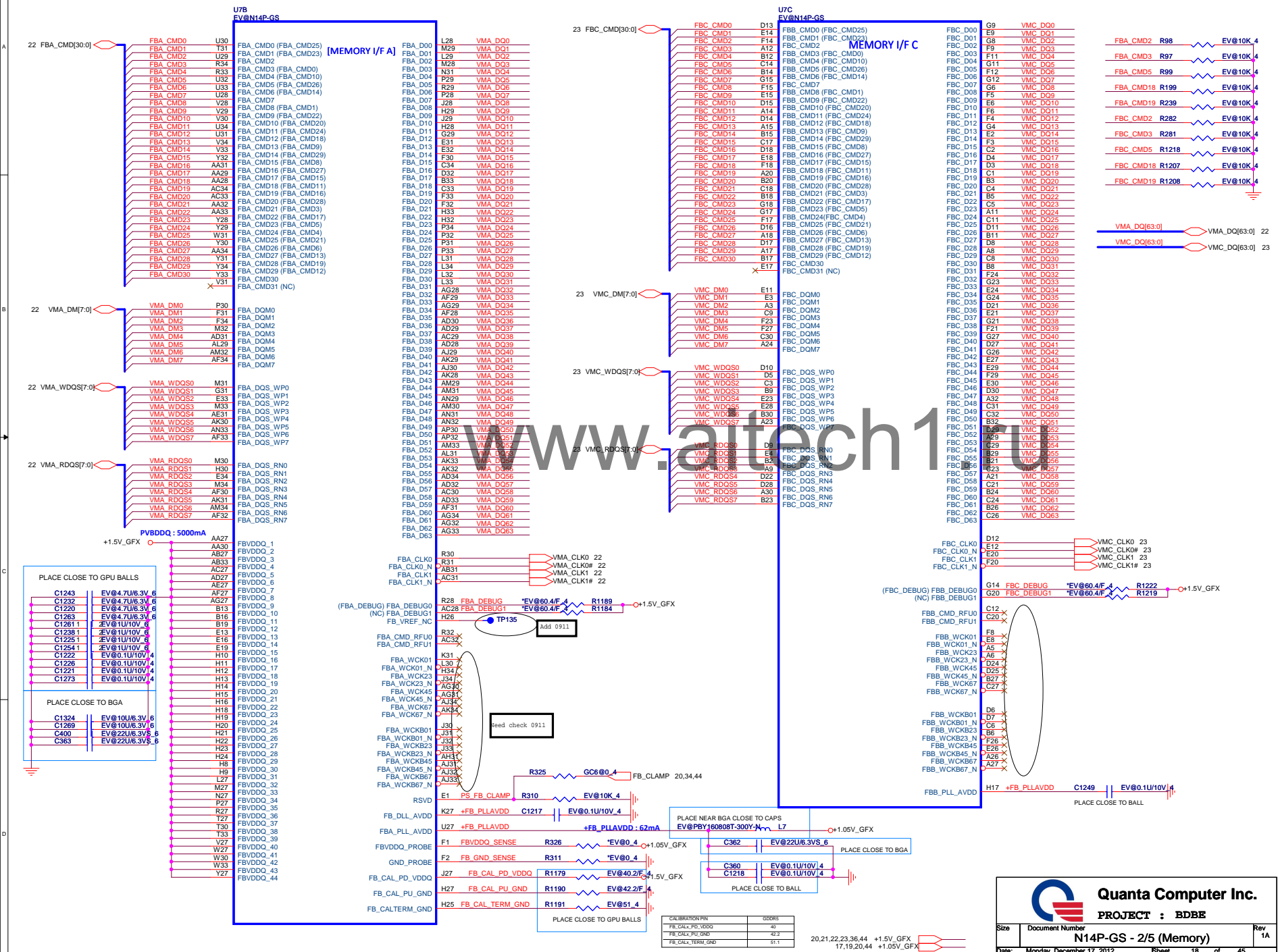
PEX_REFCLK	AL13	CLK_PCIE_VGAP	9	
PEX_REFCLK_N	AK13	CLK_PCIE_VGAN	9	
PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK	R261	EV@200_4
PEX_TSTCLK_OUT_N	AK26	PEX_TSTCLK#		
PEX_WAKE	AJ11	VGA_RST#	R1234	EV@0_4/S
PEX_RST_N	AJ12	PEX_RST#		
PEX_CLKREQ_N	AK12	PEX_CLKREQ#	R1232	EV@10K_4
PEX_TERM	AP29	PEX_TERM	R259	EV@2.49K/f
TESTMODE	AK11	TESTMODE	R1233	EV@10K_4
PEX_PLLVDD	AG26	PEX_PLLVDD	PEX_PLLVDD : 150mA	
PEX_PLL_HVDD	AH12	PEX_SVDD 3V3 : 210mA		
PEX_SVDD_3V3	AG12	EV@0.1U/10V_4	C1272	
		EV@4.7U/6.3V_4	C1325	
		EV@4.7U/6.3V_4	C1281	
3.3V_AUX_NC	P8			
VDD_SENSE	L4	VGA_VCCSENSE	43	
GND_SENSE	L5	VGA_VSSSENSE	43	

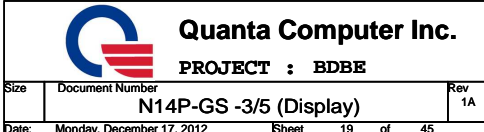


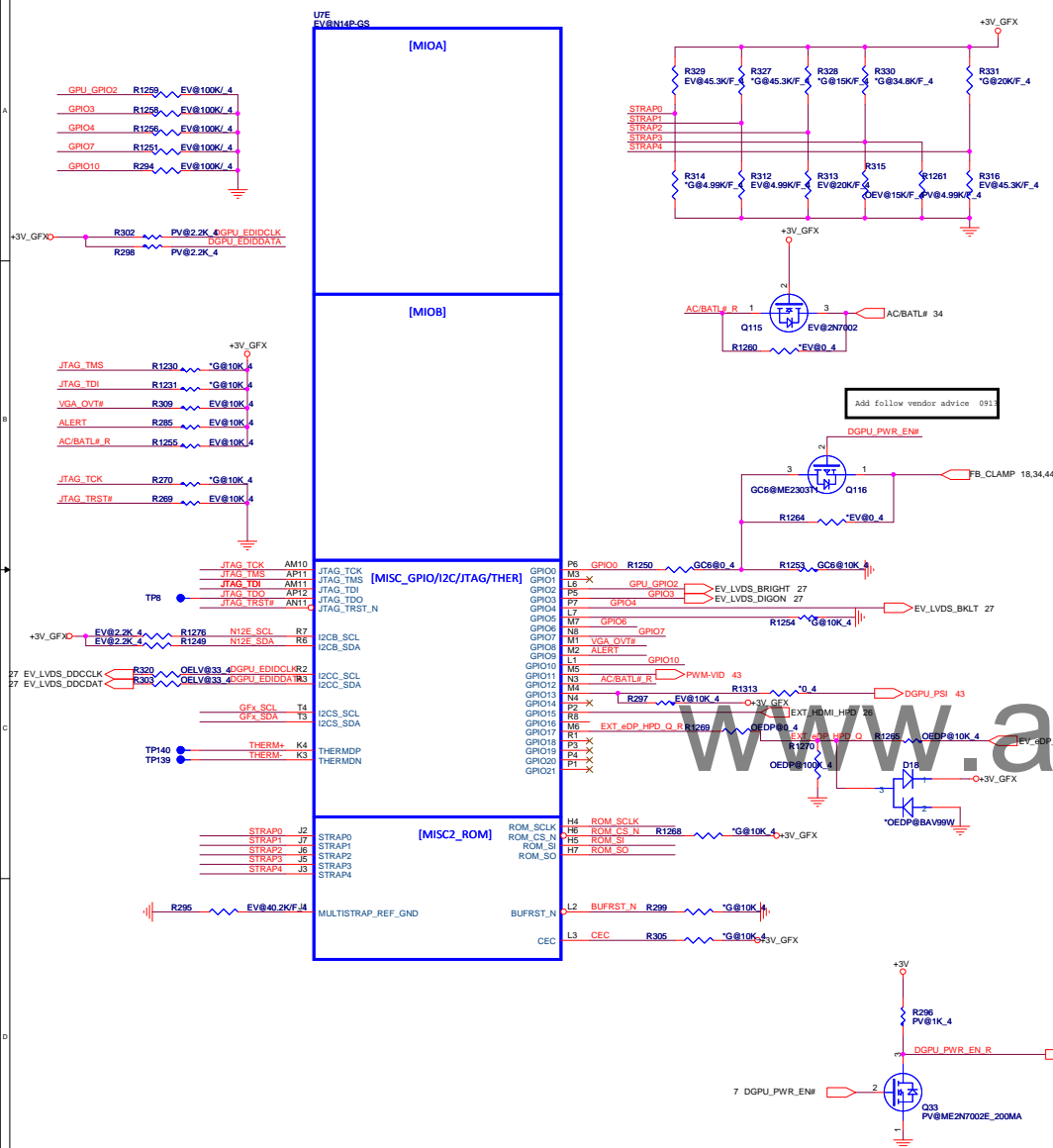
Change follow vendor advice 0913



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PROJECT : BDBE







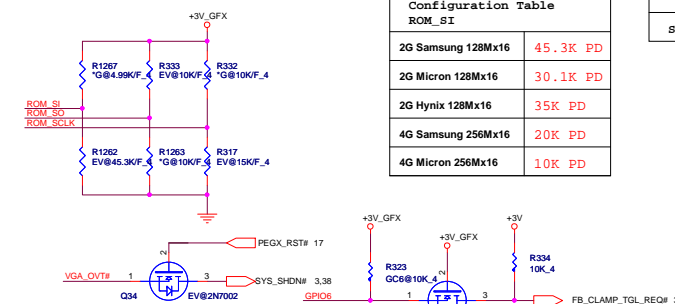
Note:

Need change the VRAM strap if used other die
 VRAM which not include by attached RVL

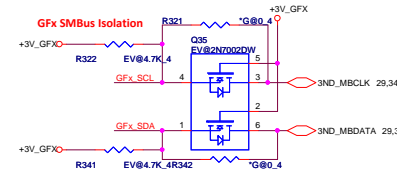
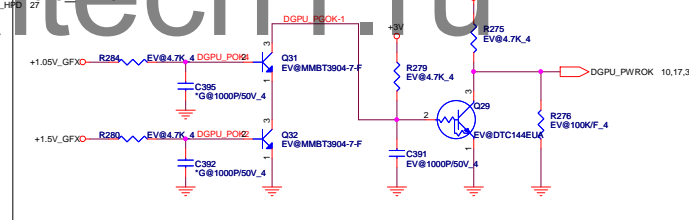
GPU	VRAM Vendor	Type	FRVDD1/FRVDD2	Config	VRAM P/N	MaxSpeed CLK	QIC Min	RAM CFG	ROM_M
N14M-GS/N14M-UP/N14P-GS2/N14P-GS3/N14P-GE	Samsung	DDR3	1.5V/1.5V	256Mx16	K9W2G16A6E-BC1A	1000MHz	1204	0x7	PD 45K
		Micro	1.5V/1.5V	128Mx16	K9W2G16A6E-BC11	900MHz	1105	0x5	PD 30K
	Hynix	DDR3	1.5V/1.5V	128Mx16	MT41J28M16JT-09G-K	1000MHz	1105	0x5	PD 30K
		Micro	1.5V/1.5V	128Mx16	MT41J28M16JT-10G-K	900MHz	1105	0x5	PD 30K
	Samsung	DDR3	1.5V/1.5V	256Mx16	K9W2G16A6E-BC1A	1000MHz	1204	0x7	PD 45K
		Micro	1.5V/1.5V	256Mx16	MT41J28M16JT-10G-K	900MHz	1105	0x5	PD 30K
N14M-GS/N14M-UP/N14P-GS2/N14P-GS3/N14P-GE	Samsung	DDR3	1.35V/1.35V	128Mx16	K9W2G16A6E-0Y11	900MHz	NA	0x6	PU 15K
		Micro	1.35V/1.35V	128Mx16	MT41J28M16JT-10G-K	900MHz	NA	0x6	PU 15K
	Hynix	DDR3	1.35V/1.35V	128Mx16	MT41J28M16JT-09G-K	1000MHz	NA	0x6	PU 15K
		Micro	1.35V/1.35V	128Mx16	MT41J28M16JT-10G-K	900MHz	NA	0x6	PU 15K
	Samsung	DDR3	1.35V/1.35V	128Mx16	K9W2G16A6E-0Y11	900MHz	NA	0x6	PU 15K
		Micro	1.35V/1.35V	128Mx16	MT41J28M16JT-10G-K	900MHz	NA	0x6	PU 15K

VRAM (DDR3L / 900MHz)	Configuration Table
ROM_S1	
2G Samsung 128Mx16	15K PU
2G Micron 128Mx16	5K PU

Default: SAM 2G VRAM	
VRAM (DDR3 / 1000MHz)	Configuration Table
ROM_S1	
2G Samsung 128Mx16	45.3K PD
2G Micron 128Mx16	30.1K PD
2G Hynix 128Mx16	35K PD
4G Samsung 256Mx16	20K PD
4G Micron 256Mx16	10K PD



GPU_PWR0K



N14P-GS ID:

Netname	N14P-GS
ROM_SO	OP 5K PU GS 10K PU
ROM_SCLK	15K PD
STRAP0	45K PU
STRAP1	5K PD
STRAP2	20K PD
STRAP3	GS:15K PD OP:5K PD
STRAP4	45K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB26 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB26 RES CHIP 20K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

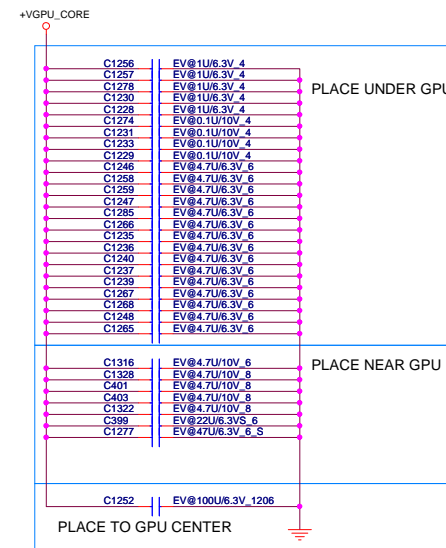
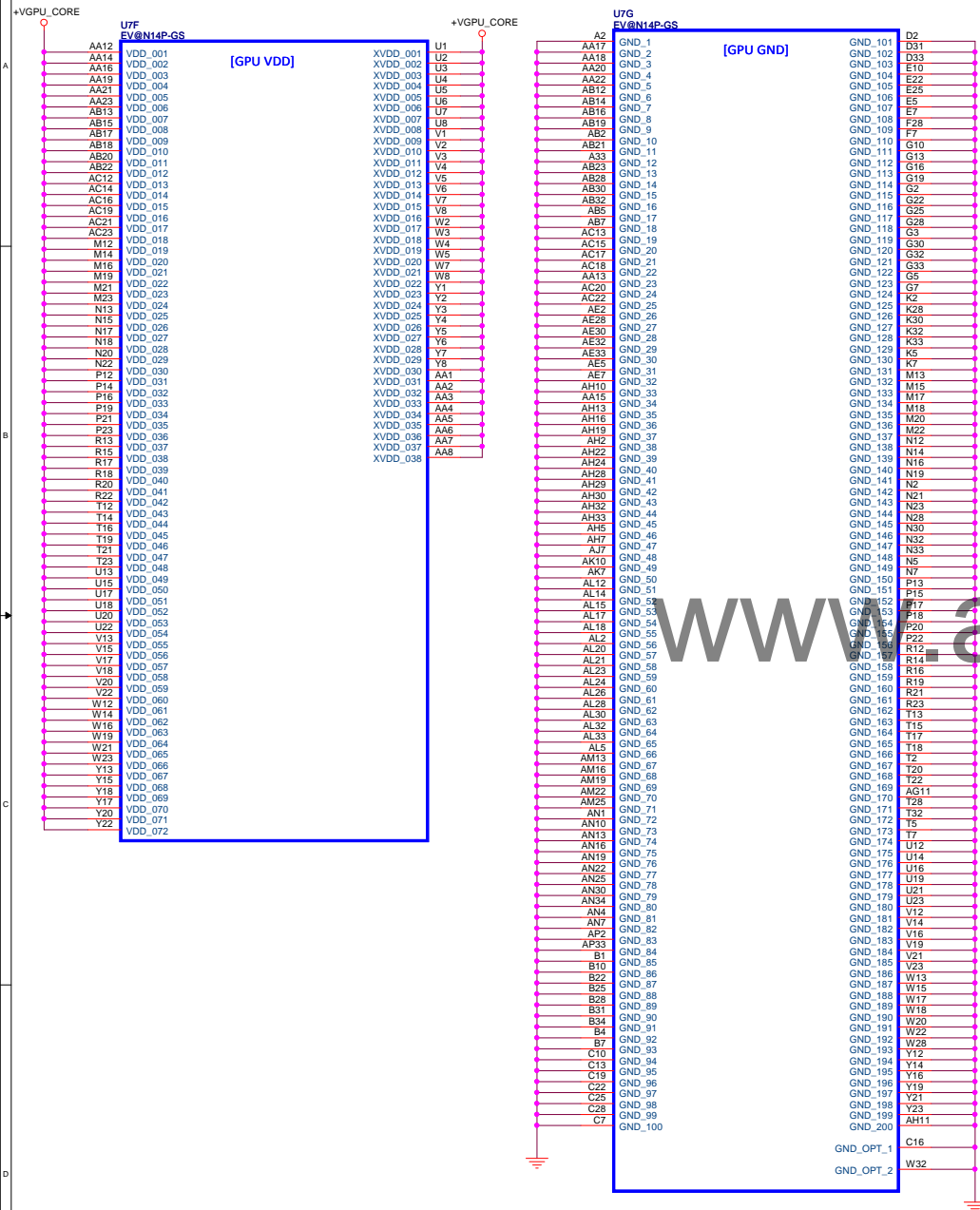
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PC1_DEV0[4]	SUB_VENDOR	PC1_DEV0[3]	PEX_PLU_EN_TERM
ROM_S1	RAM_CFG[4]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	FB[1]	FB[0]	SMBALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3G0_PADCFG[3]	3G0_PADCFG[2]	3G0_PADCFG[1]	3G0_PADCFG[0]
STRAP2	PC1_DEV0[3]	PC1_DEV0[2]	PC1_DEV0[1]	PC1_DEV0[0]
STRAP3	S0B3_EXPOSED	S0B2_EXPOSED	S0B1_EXPOSED	S0B0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHARGE_GEN3	PCIE_MAX_SPEED	DP_PLU_VDD33V

GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVDD PWM1_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVDD PWM1_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

VDD/XVDD : 25.72A



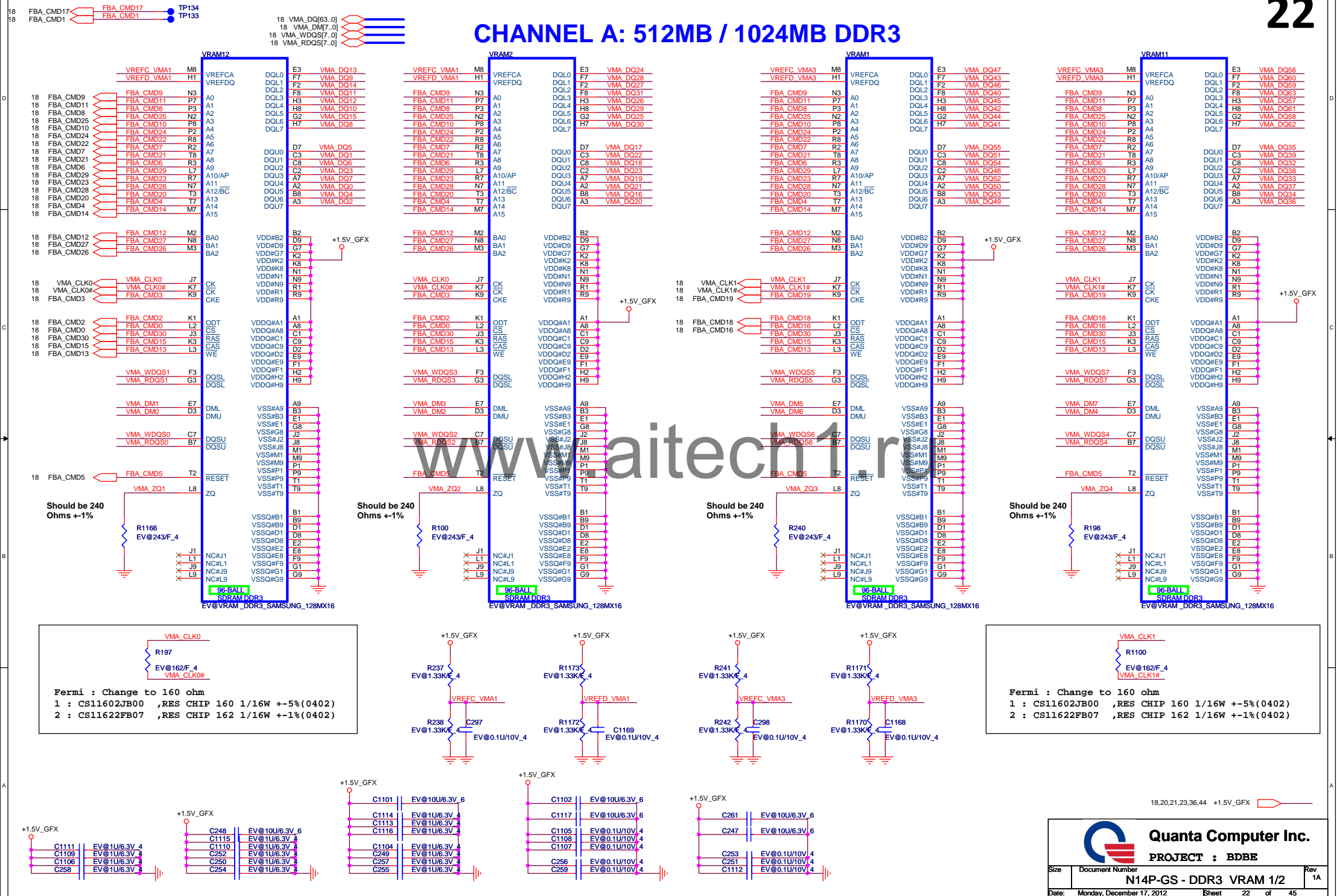
for meet Power down sequence for +3V_GFX



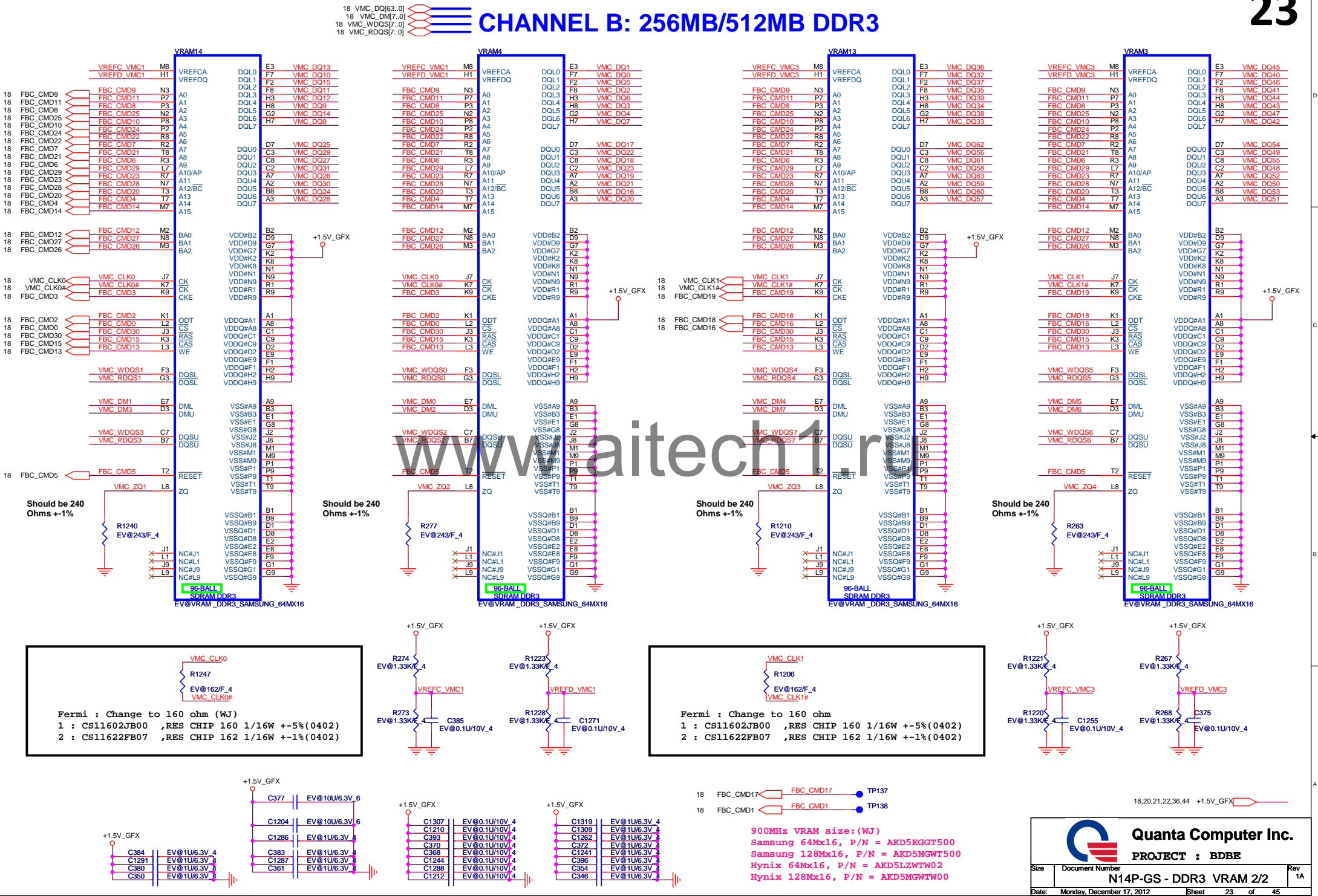
B2A

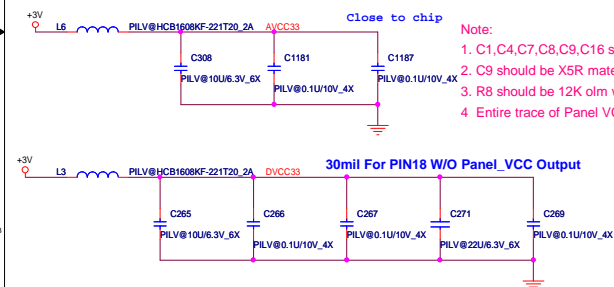
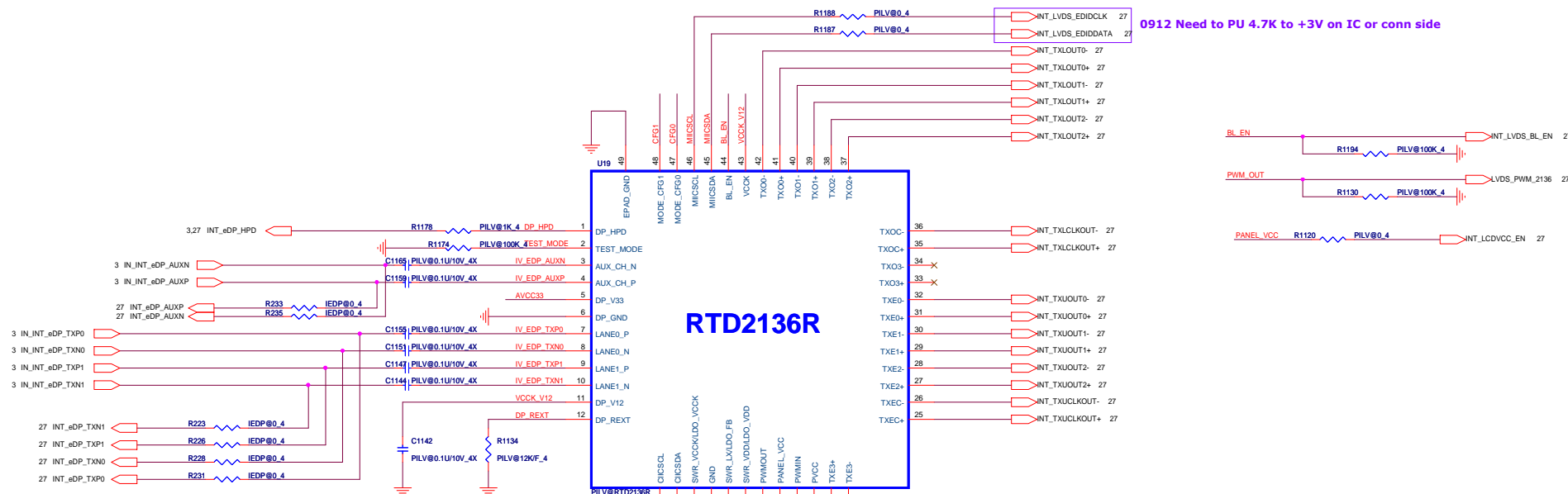
120808 Del DGPU_PWROK circuit
because all +1.05V_GFX/+1.5V_GFX
power solution have PG connector
to PCH

CHANNEL A: 512MB / 1024MB DDR3



CHANNEL B: 256MB/512MB DDR3





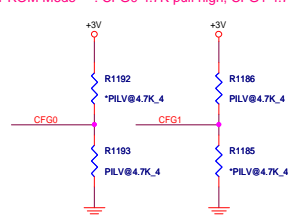
Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high

EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low

EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high

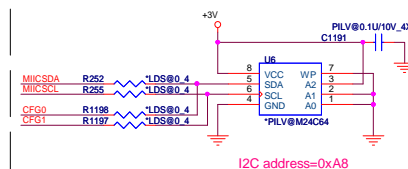


EEPROM Mode

In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following condition.

- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

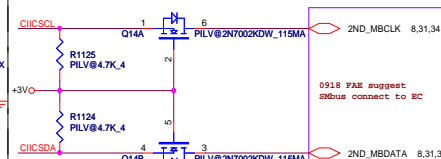
- **State address errors converge as time**



EP Mode

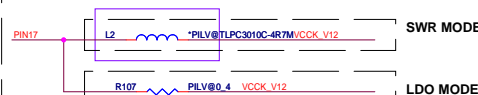
External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used

Address=0x94&0x6A

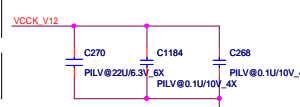


Dual Mode Regulator Configuration

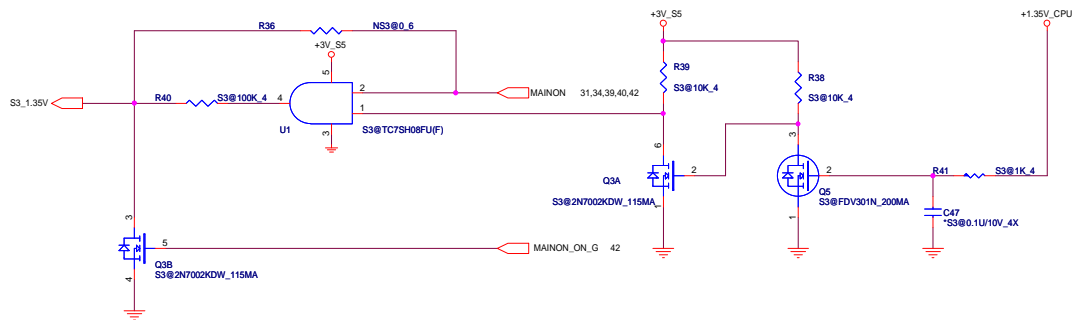
	2.2-uH(L6)	0 Ohm(R31)
SWR	Connect	NC
LDO	NC	Connect



1. C18 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17

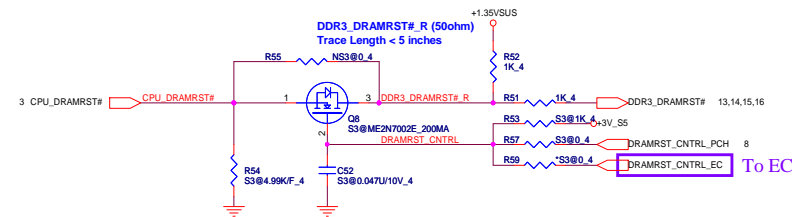


For S3 power Reduction Sequence S3P/NS3P/CPU

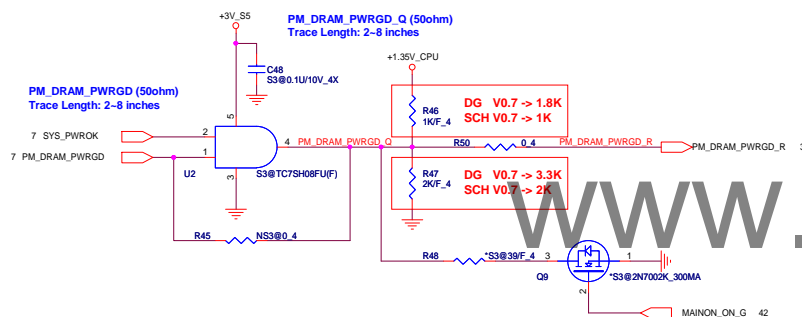


SM_DRAMRST# Topology S3P/NS3P/CPU

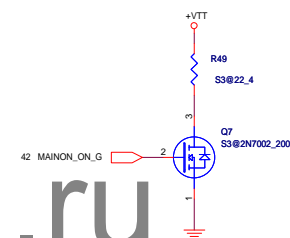
25



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

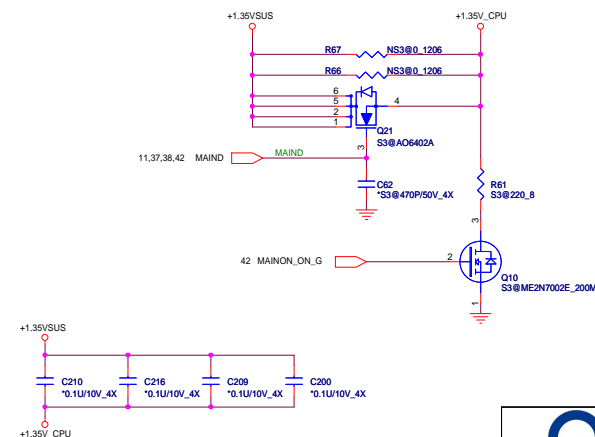


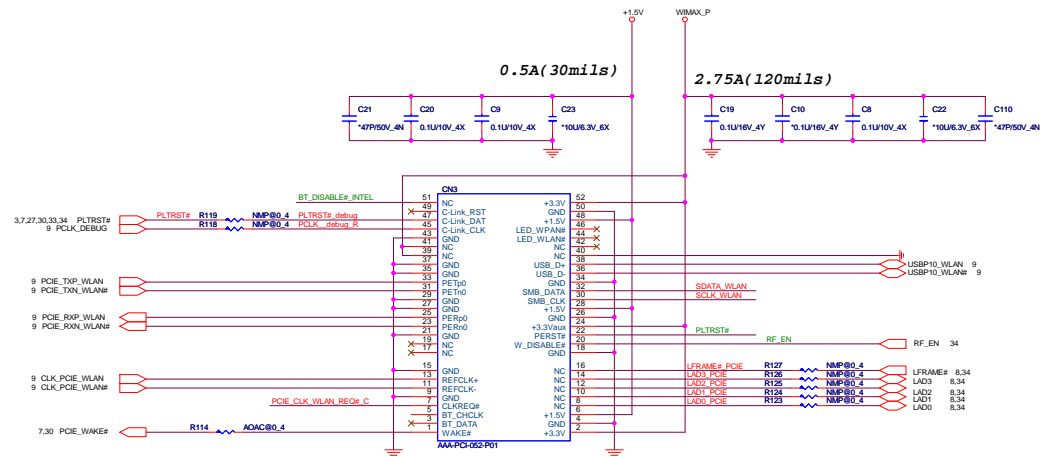
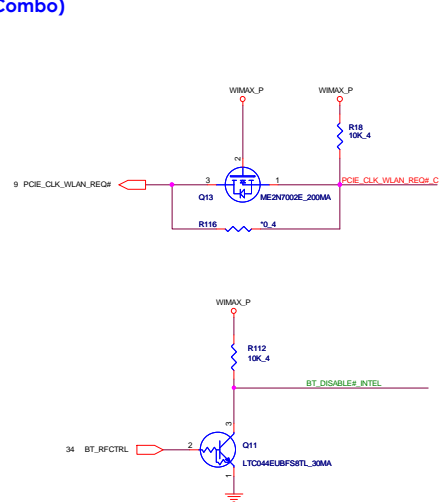
For S3 power Reduction VTT discharge S3P/NS3P/CPU



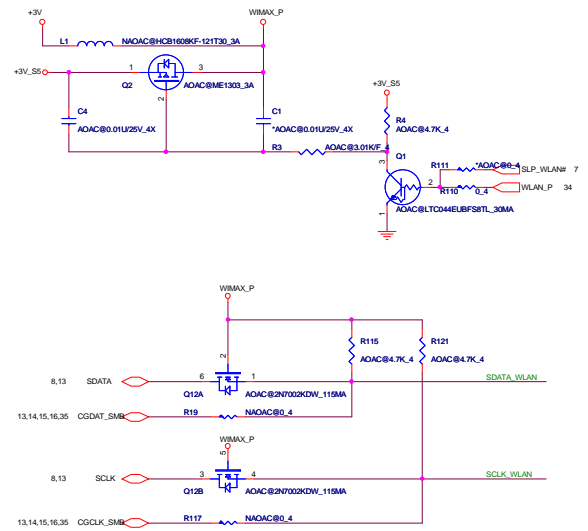
CPU SM_VREF S3P/NS3P/CPU

S3 power Reduction (CPU Power) S3P/NS3P/CPU





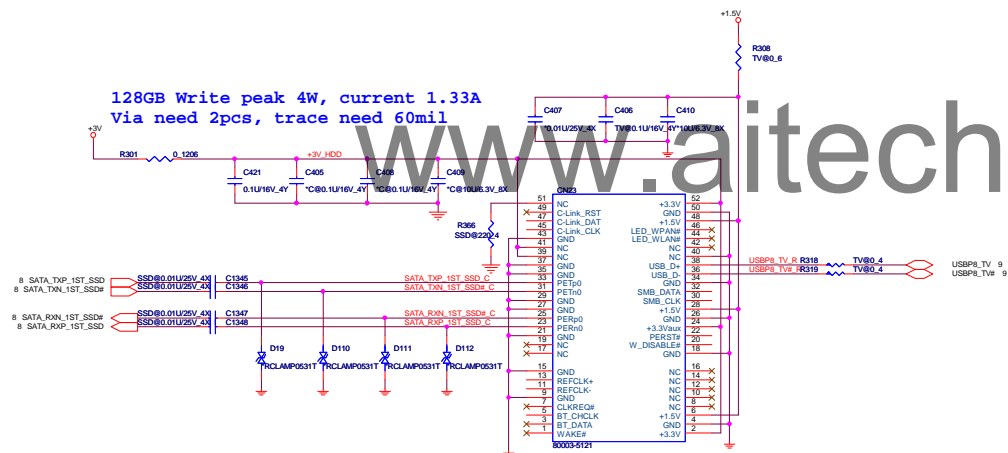
[AOAC]



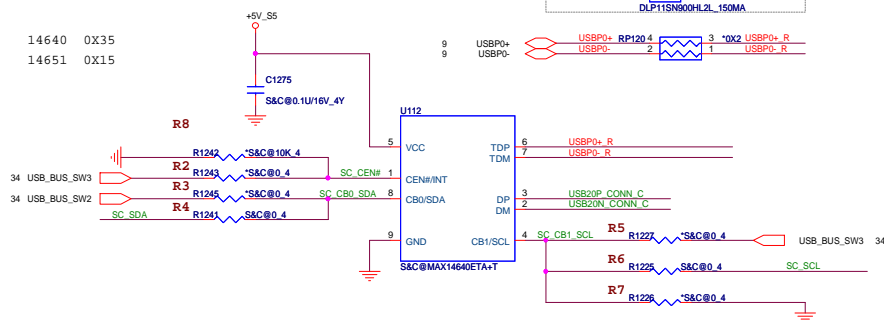
TV Tuner / MSATA

<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



USB CONNECT <U3B/USB>
RIGHT(UR)



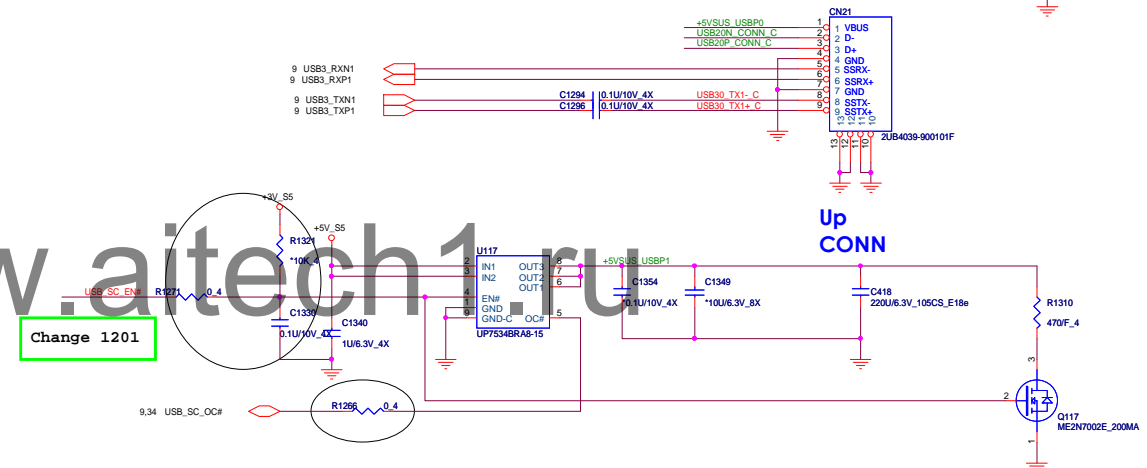
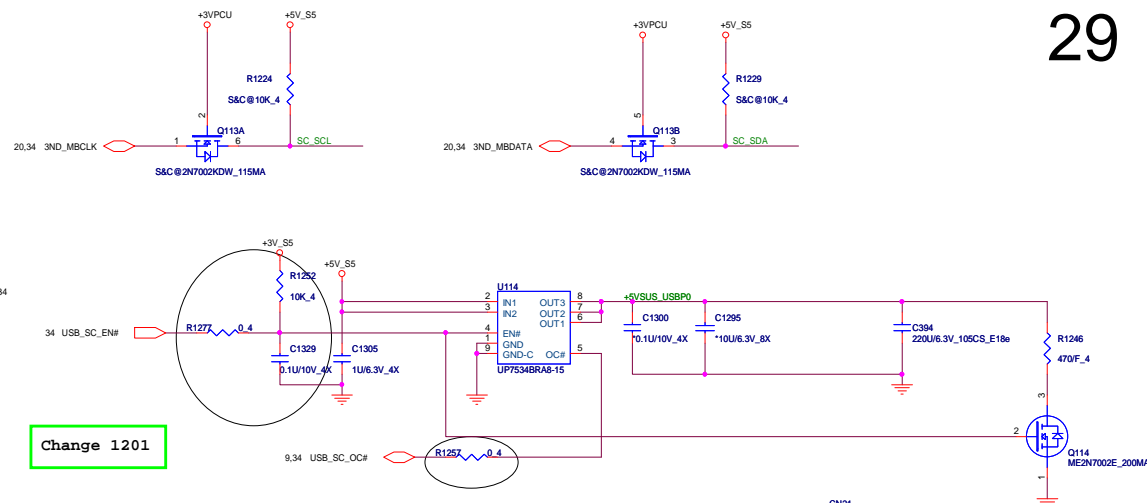
	R1	R2	R3	R4	R5	R6	R7	R8
14566		V	V				V	
14600			V		V			
14617(with CB2)	V		V		V			
14617(no CB2)			V		V			V
14641/42/44			V		V			
14640				V		V		

SW2	SW3	14600
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	0	Pass-Through(USB) mode
1	1	Pass-Through(USB) mode with CDP Emulation

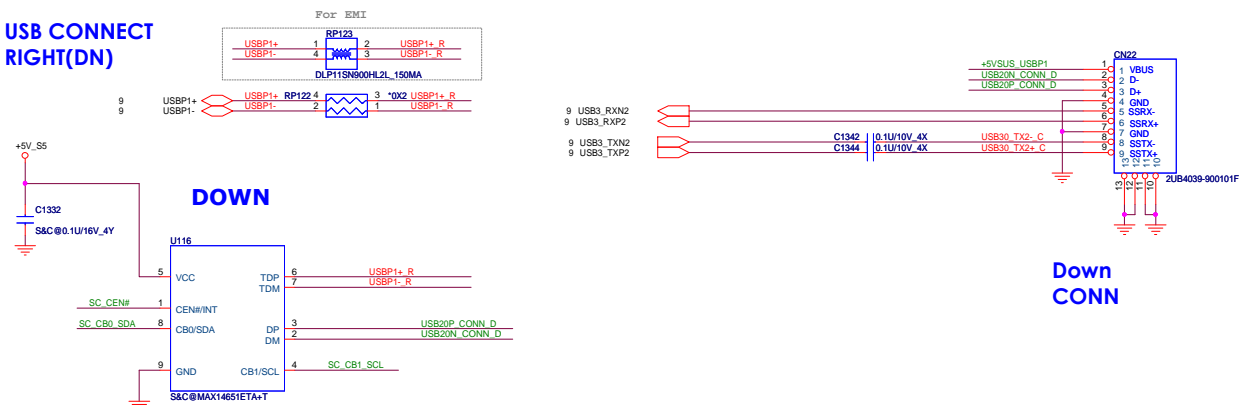
SW2	SW3	14644
CB0	CB1	Status
0	0	2A Auto mode for Apple Device
1	0	Force dedicated charger mode
0	1	Pass-Through(USB) mode
1	1	Pass-Through(USB) mode with CDP Emulation

SW2	SW3	14641
CB0	CB1	Status
0	0	2A Auto mode for Apple Device
1	0	Force 1A for Apple Device
0	1	Pass-Through(USB) mode
1	1	Pass-Through(USB) mode with CDP Emulation

SW2	SW3	14642
CB0	CB1	Status
X	0	2A Auto mode for Apple Device
0	1	Pass-Through(USB) mode
1	1	Pass-Through(USB) mode with CDP Emulation

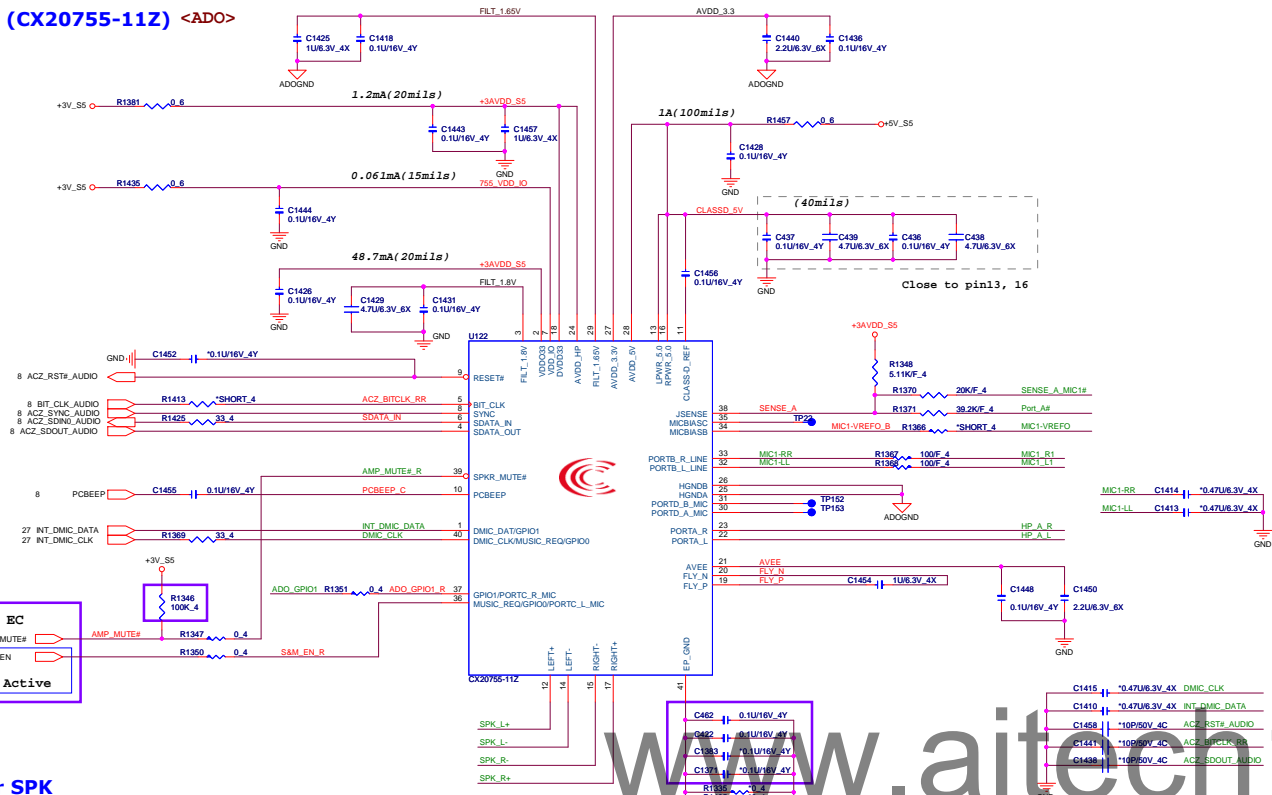


USB CONNECT
RIGHT(DN)

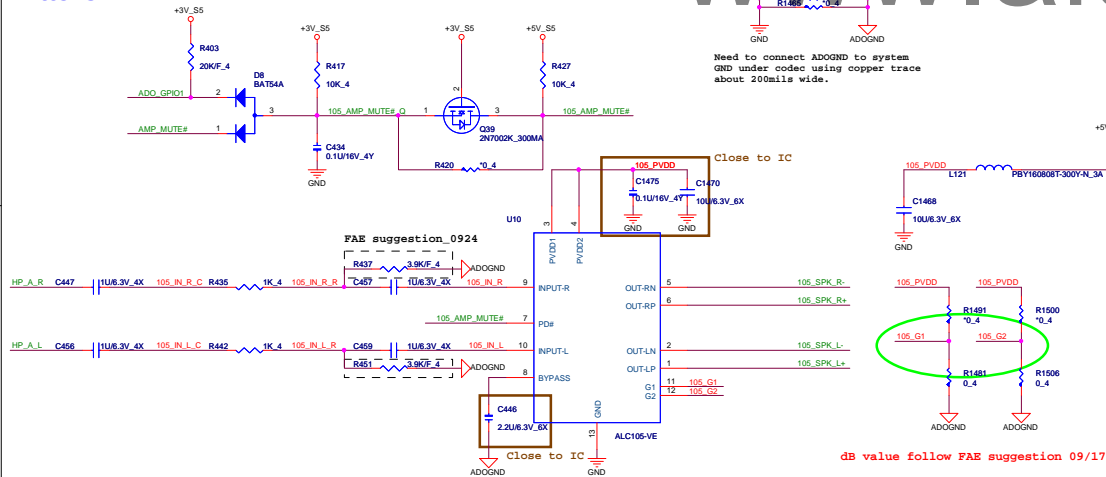




Codec (CX20755-11Z) <ADO>



Twitter SPK

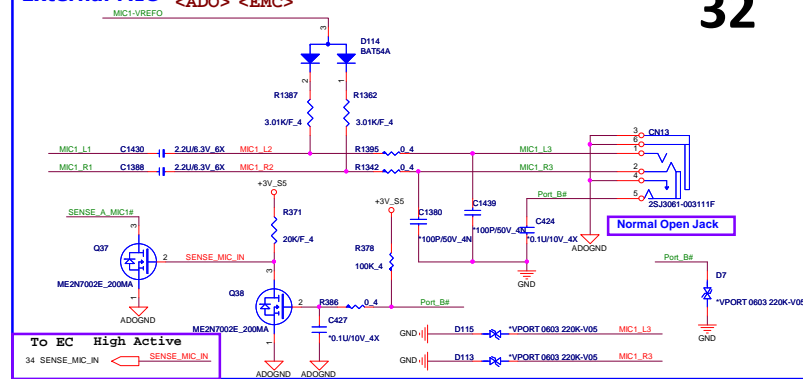


Output Gain Table

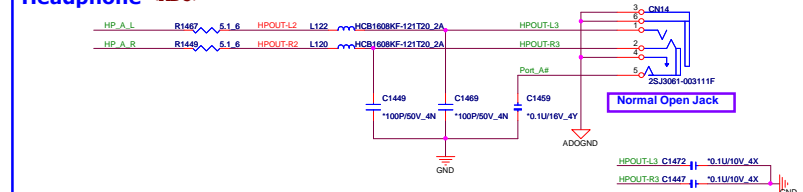
G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

dB value follow FAE suggestion 09/17

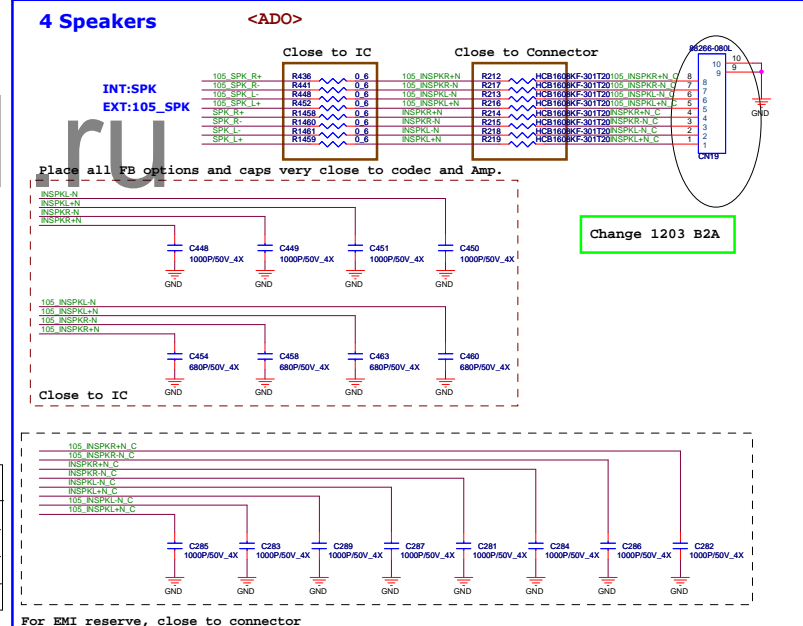
External MIC $\langle ADO \rangle \langle EMC \rangle$



Headphone <ADO>



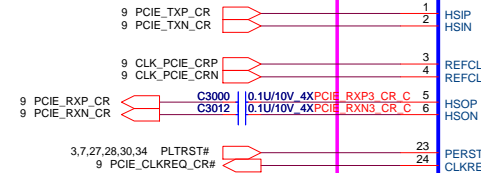
4 Speakers



For EMI reserve, close to connector

Change interface from USB3.0 to PCIe

A1A



RT5229

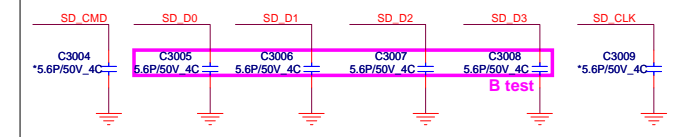
EMI solution

Close to chip pin

Share Pin

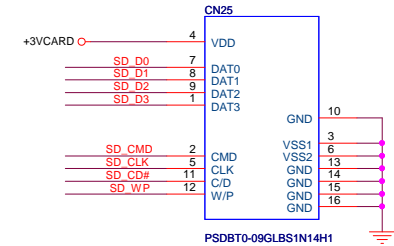
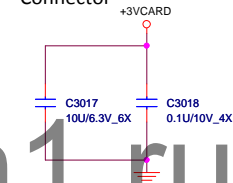
EMI Solution

Please help to close to connector



SD / MMC

CARD READER

Place close to
Connector

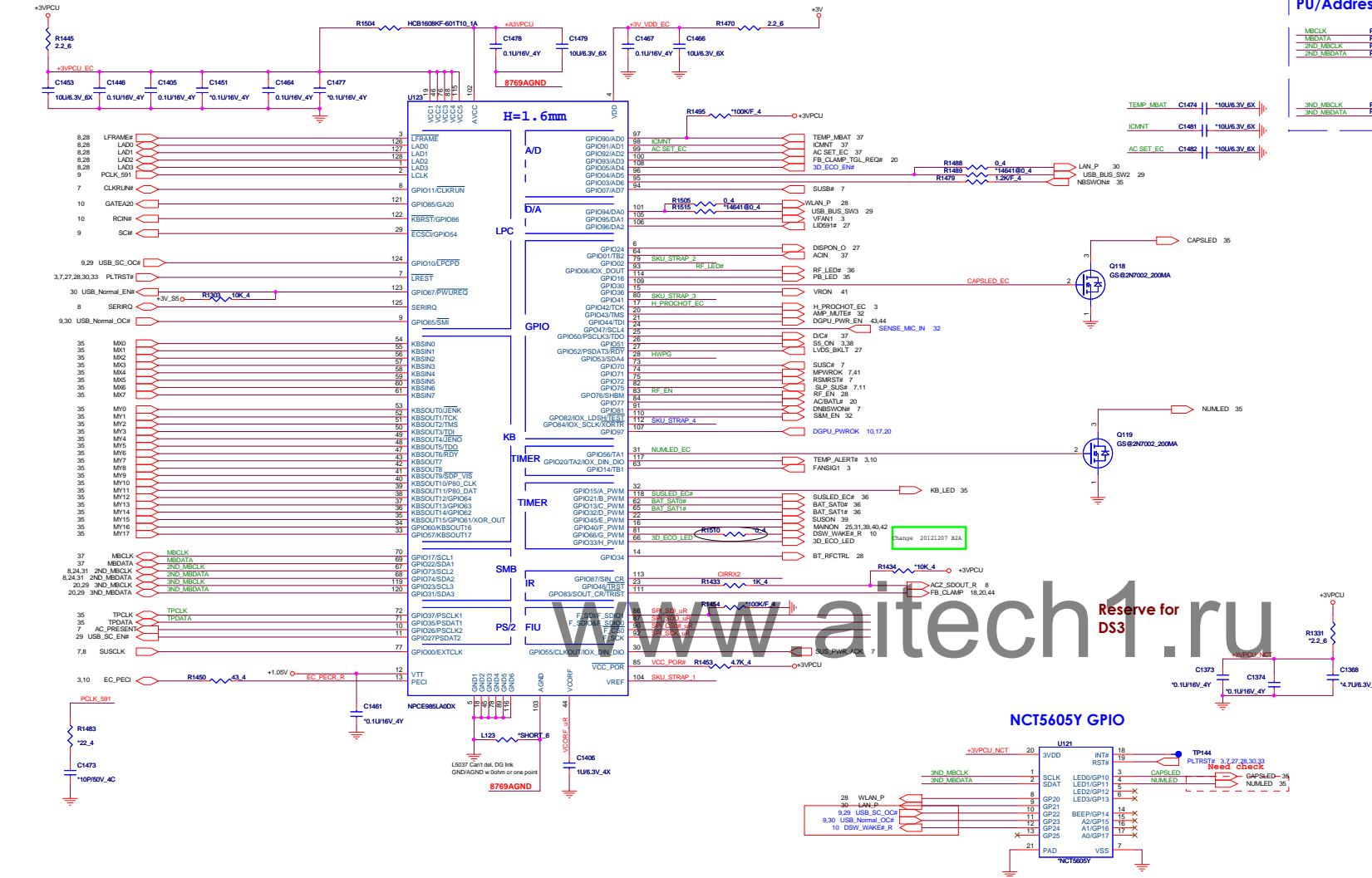
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PROJECT : BDBE

Size	Document Number	Rev
	Card Reader(AU6437)	1A
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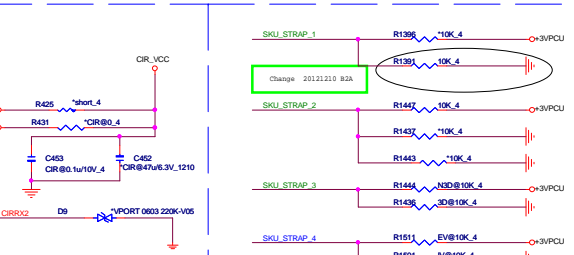
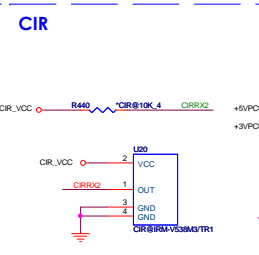
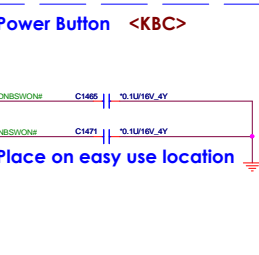
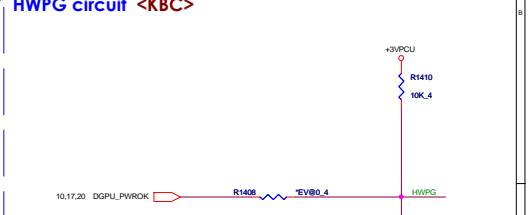
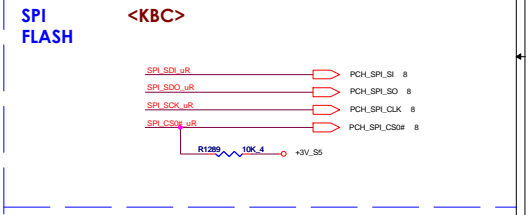
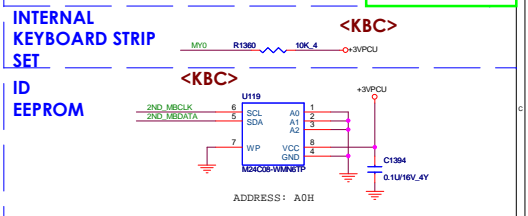
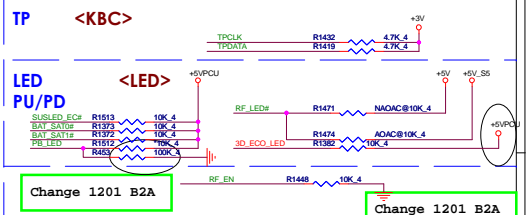


SM BUS PU/Address

SM BUS PU/Address	Value
MBCLK	R1415 4.7K 4
MBDATA	R1416 4.7K 4
2ND MBCLK	R1398 4.7K 4
2ND MBDATA	R1399 4.7K 4

SMBUS Devices

Devices	Address
Battery(A)	
PCH(SS)	
G-sensor(S0)	
IDROM(A)	
EDP2LVDS IC	94H or 64H
VGA Thermal(A or S0)	98H
Extend GPIO	
S&C IC 14640 Up Port	35H
S&C IC 14651 Down Port	15H



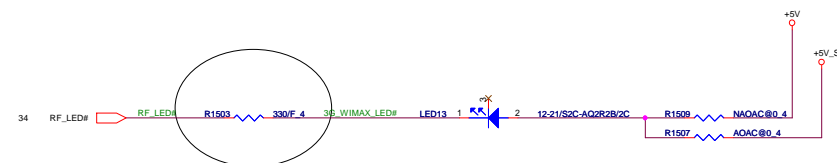
MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17" P	0			
17" G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optimus)				1

[illegible][illegible]

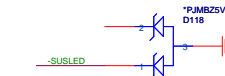
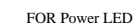
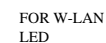
Change 12/05 B2A

88286-04CL

[illegible][illegible]

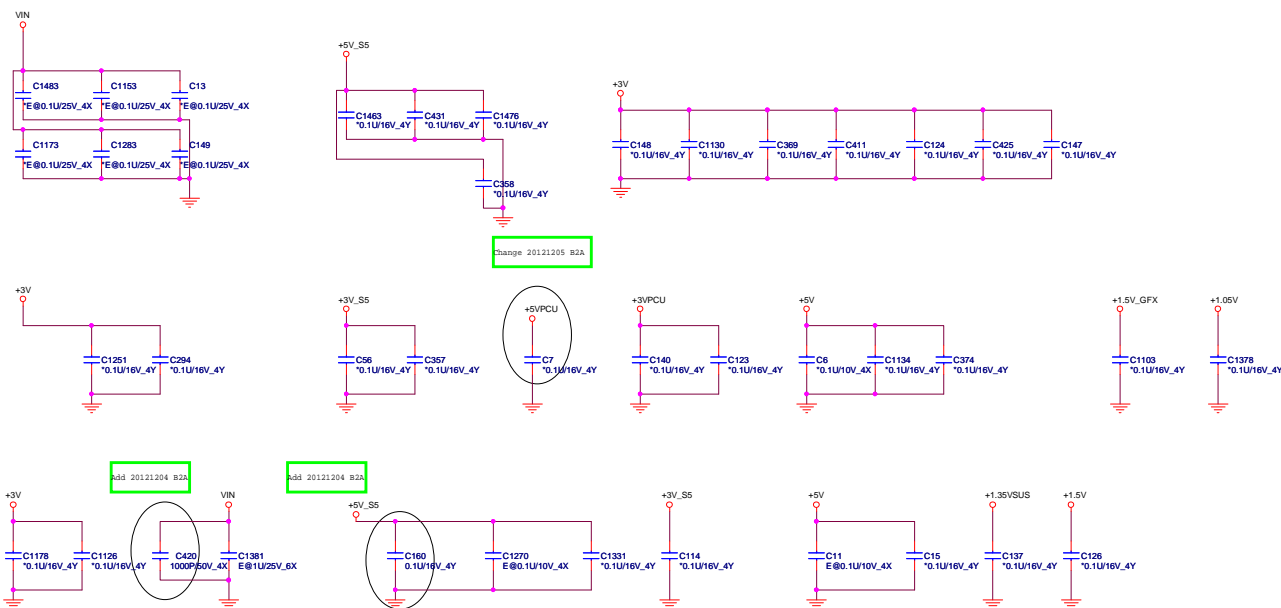


POWER LED



EMI EMI

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ADD

Follow BD6
Sky 09/24





Change enable signal from
SUSON to be MAINON for EE
just need 1.05V S0 power
09/27 Sky

Change for OCP setting
10/19 Sky

PR1120
78.7K/F_4

PC1150
1U/6.3V_4X

PU18 TPS51211DSCR
V5IN
TRIP
EN
VFB
TST
GND
GND
GND
GND
GND
GND
GND
GND

PR1114 2.2_6
PC1149 0.1U/25V_6X

PQ24
AON7410

PC1137
0.1U/25V_4X

PC1142
10U/25V_8X

PC1144
*EV@2200P/50V_4X

Follow EMI
9/25 Sky

OCP:8A

(Peak 6.523A, AVG 4.566A)

Total capacitor : 400uF

F: 320k Hz

+1.05V

PL9
2.2UH_7X7_TOK

HWP_1.05V 34
+3V_S5

*10K_4 PR90

RDSon=13m ohm

PQ25
AON7752

PR1110
*2.2/F_6

PC1145
*1000P/50V_4X

(Near by Output
cap side)

$$V_{out} = 0.704V * (R1 + R2) / R2$$

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Delete PQ5064, PC405, PJP7 for EE
just need 1.05V S0 power 09/27 Sky

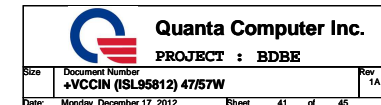


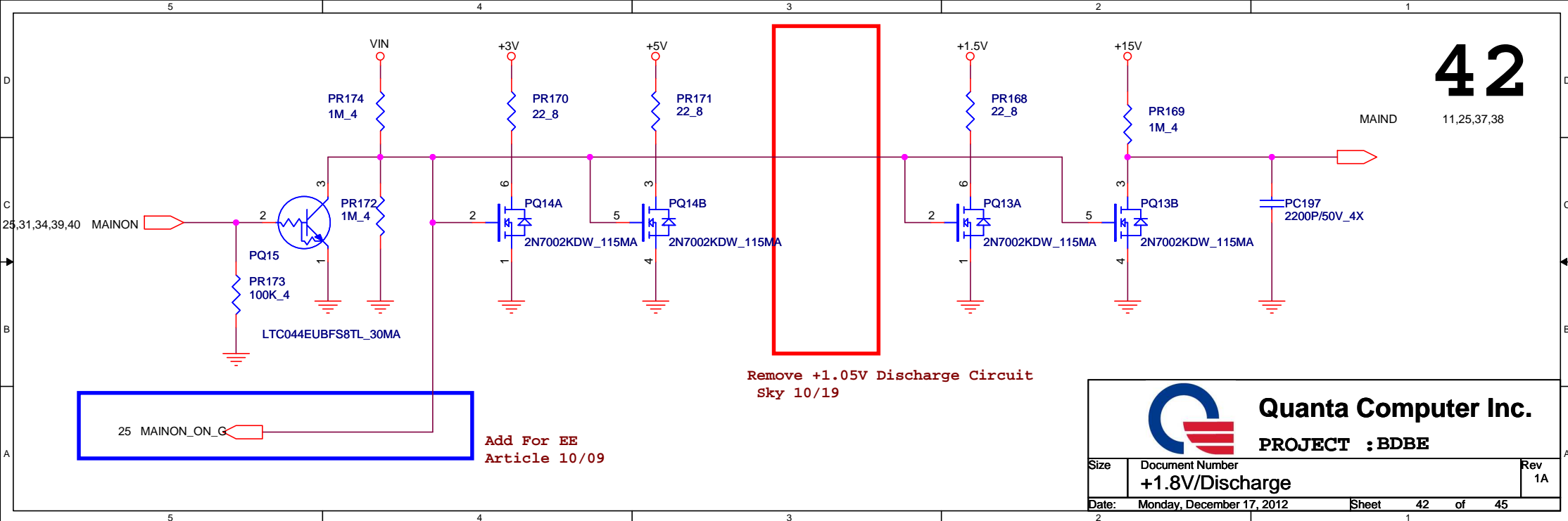
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PROJECT : BDBE

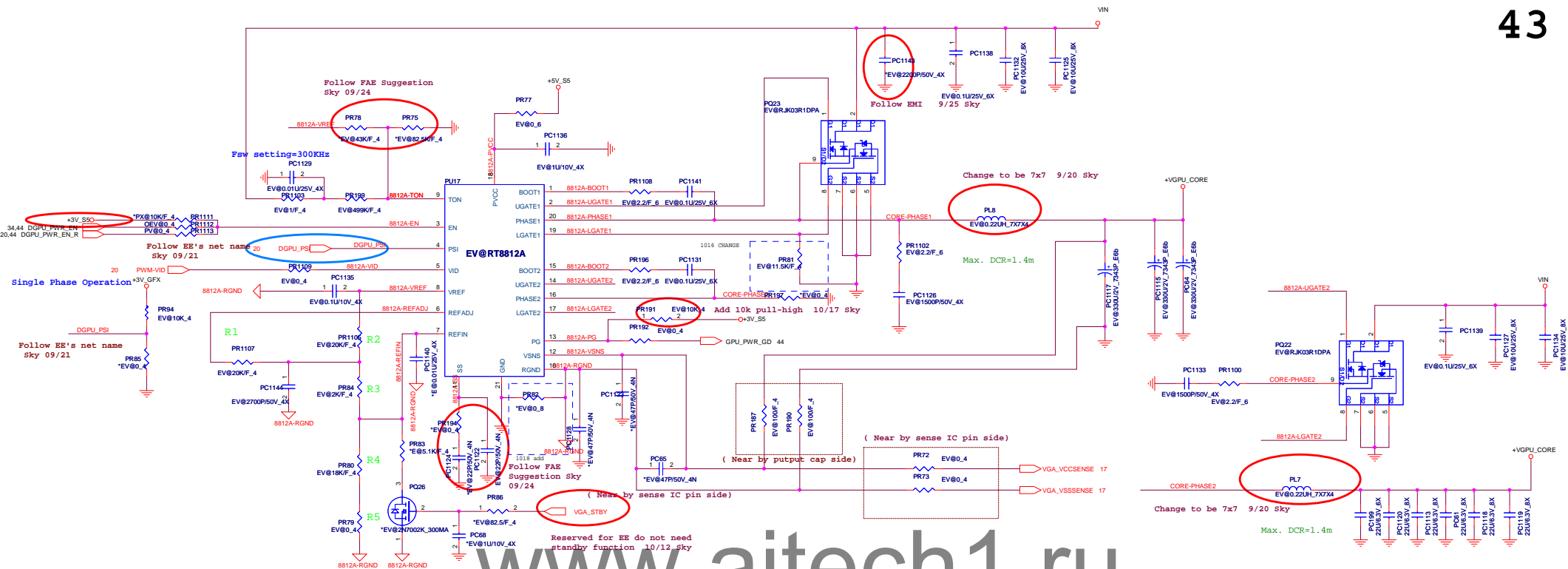
Size	Document Number	Rev
	+1.05V_A(TPS51211DSCR)	1A
Date:	Monday, December 17, 2012	Sheet 40 of 45

OCP = 66A

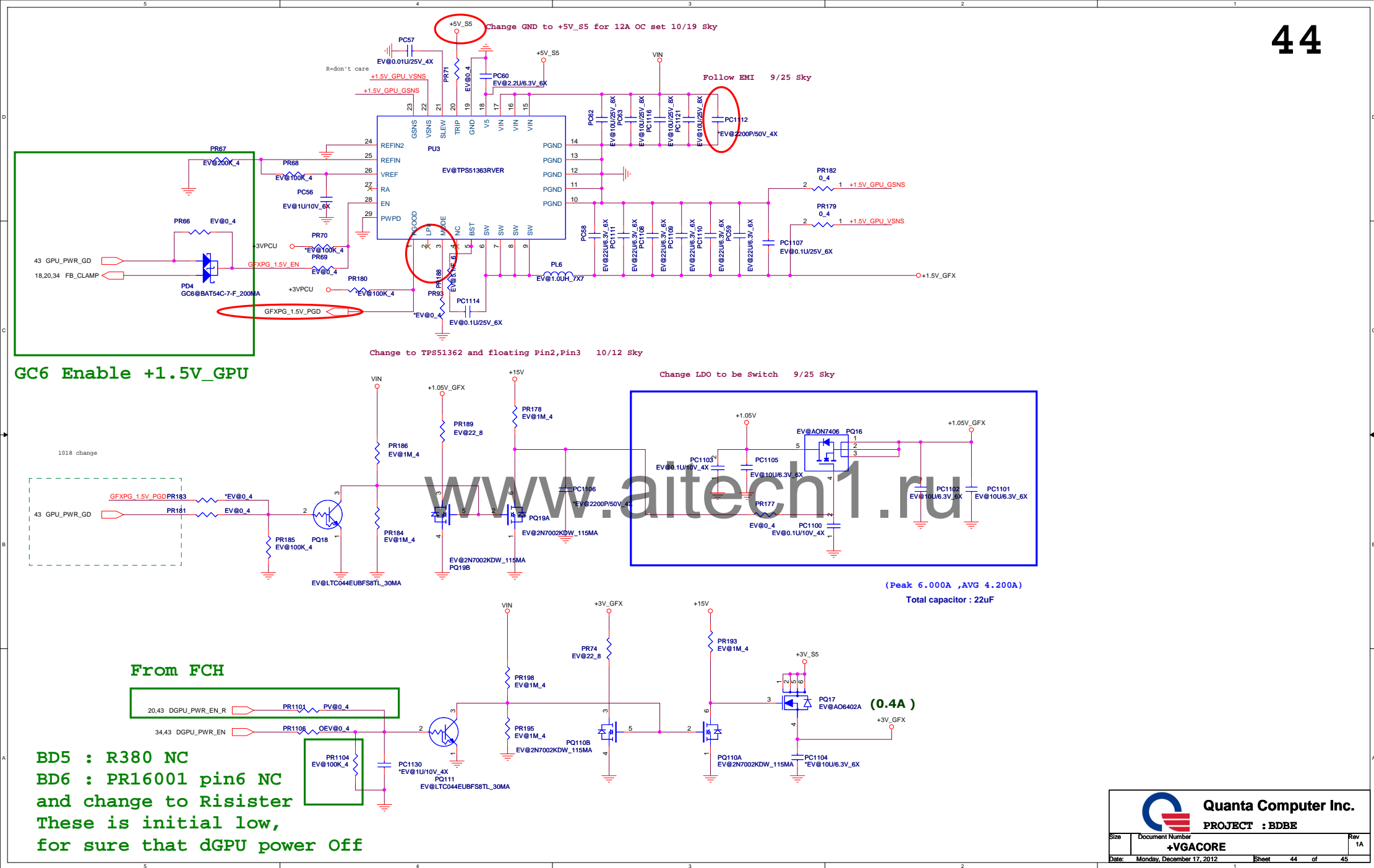




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PROJECT : BDBE

Size	Document Number	Rev
	+VGACORE	1A
Date: Monday, December 17, 2012	Sheet 44 of 45	

Model	REV	CHANGE LIST	MODEL			BDB		
			PAGE	FROM	To			
BDB	B2A	PAGE 8: C445,C455 Change to 15pf PAGE 8: CN7 Change to socket type PAGE 8: Add R1328 and R1516 for QUAD IO PAGE 9: Change C419, C423 to 12pf PAGE 10: Add board ID for SPK,CIR,TV PAGE 11: Change R1339 to +3v_s5 for EC code PAGE 19: Change C397,C398 to 12pf PAGE 30: Add LAN IC PAGE 32: Change R212,R213,R214,R215,R216,R217,R218,R219 to bead PAGE 33: Change Cardreader to RTS5229 PAGE 33: Add R453 for PB_LED change to high active PAGE 34: Remove R1408 for optimus PAGE 35: Change PWR/B LED PWR to +5VPCU for white LED PAGE 35: Change hole1,hole2,hole112 and hole117 for ID PAGE 36: Change R1496,R1497,R1499 and R1503 for LED brightness SPEC				1	1A	
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DOC NO. 204		PROJECT MODEL :	BDB	APPROVED BY:		DATE:		<div> Quanta Computer Inc. PROJECT : BDBE</div> <div>Change list</div> <div>Date: Monday, December 17, 2012 Sheet 49 of 49</div>
		PART NUMBER:		DRAWING BY:		REVISION:		